RX26T Group

Renesas MCUs

R01DS0407EJ0110
Rev.1.10
Aug 10, 2023

120-MHz, 32-bit RX MCU, on-chip FPU, 709 CoreMark, Supportive of 5V power supply, up to 512-KB flash memory, up to 64-KB SRAM, 16-KB data flash memory, various communications interfaces including CAN FD, Simultaneous sampling with 3 units of 12-bit A/D converter (up to 7 channels), Analog comparator (6 channels), 120 MHz PWM (4 channels for 3-phase complementary, 2 channels for 5-phase complementary, 10 channels for single-phase complementary), 4-channel high-resolution PWM with resolution of 260 ps at the minimum, Encryption functions

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 120 MHz
  Capable of 709 CoreMark in operation at 120 MHz
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Operation from a single 2.7- to 5.5-V supply
- Three low-power modes

■ On-chip code flash memory
- Supports versions with up to 512 Kbytes of ROM
- Operation at 120 MHz (with no waiting)
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

■ On-chip data flash memory
- 16 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM
- 64 K/48Kbytes of SRAM (with no waiting)

■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel

■ ELC
- Module operation can be initiated by event signals without using interrupts
- Linked operation between modules is possible when the CPU is in sleep mode

■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

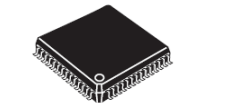
■ Clock functions
- The main clock oscillator is connectable to an 8- to 24-MHz external crystal resonator and usable as the PLL reference clock.
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Independent watchdog timer
- 120-kHz IWDT-dedicated on-chip oscillator clock operation

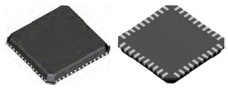
■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, functions for self-diagnosis and detection of disconnection for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test-assisting function by DOC, and CRCA, etc.
- Register write protection function can protect values in important registers against overwriting.

■ Encryption functions (Trusted Secure IP Lite)
- 128- or 256-bit key length of AES for ECB, CBC, GCM, others
- True random number generator
- Unauthorized access to the encryption engine is disabled and imposture and falsification of information are prevented
- Safe management of keys

■ Up to 83 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability, and retention of the port output



PLQP0100KB-B 14 × 14 mm, 0.5 mm pitch
PLQP0080KB-B 12 × 12 mm, 0.5 mm pitch
PLQP0064KB-C 10 × 10 mm, 0.5 mm pitch
PLQP0048KB-B 7 × 7 mm, 0.5 mm pitch



PWQN0064KF-A 9 × 9 mm, 0.5 mm pitch
PWQN0048KC-A 7 × 7 mm, 0.5 mm pitch

■ Various communications interfaces
- CAN FD: Compliant with ISO11898-1:2015, standard frame and extended frame (1 channel)
- SCIk and SCIh with multiple functionalities (up to 4 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- Up to three RSCIs with Manchester encoding and HBS functionality
- I^2C bus interface (RIICa) for transfer at up to 400 kbps (fast mode), capable of SMBus operation (1 channel)
- I3C bus interface (RI3C) for the single data rate (SDR) mode (1 channel)
- RSPId (1 channel) for transfer at up to 30 Mbps

■ Up to 29 extended-function timers
- 32-bit (products with 64 Kbytes of RAM) or 16-bit (products with 48 Kbytes of RAM) GPTWa (8 channels): operation at 120 MHz, input capture, output compare, PWM waveforms: 10 output channels in single-phase complementary PWM mode/3 output channels in 3-phase complementary PWM mode/2 output channels in 5-phase complementary PWM mode, phase-counting mode, linkage with comparator (counting operation, PWM negate control)
- 16-bit MTU3d (9 channels): operation at 120 MHz, input capture, output compare, PWM waveforms: 2 output channels in 3-phase complementary PWM mode, phase-counting mode
- 8-bit TMRb (8 channels)
- 16-bit CMT (4 channels)

■ High-resolution PWM waveform generation circuit (HRPWM): 4 channels
- Controlling the timing of rising or falling of the PWM output waveform for 32-bit GPTWa is realized with minimum of 260 ps resolution (in operation at 120 MHz)

■ 12-bit A/D converter (S12ADH)
- Products with 64 Kbytes of RAM
  Three 12-bit units of sample-and-hold circuit included:
  Unit 0 (4 channels for 3 sample-and-hold circuits),
  Unit 1 (4 channels for 3 sample-and-hold circuits),
  Unit 2 (14 channels)
- Products with 48 Kbytes of RAM
  Two 12-bit units of sample-and-hold circuit included:
  Unit 0 (7 channels for 3 sample-and-hold circuits),
  Unit 2 (8 channels)

■ Analog Comparator (CMPCa): 6 channels

■ 12-bit D/A converter: 2 channels
- Usable as a reference voltage for the analog comparator

■ Temperature sensor for measuring temperature within the chip

■ Recommended operating temp. range (Topr)
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 shows the outline of maximum specifications. The peripheral functions and the number of their channels vary depending on the number of pins of the package, and the RAM capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • 113 instructions (products with 64 Kbytes of RAM), 111 instructions (products with 48 Kbytes of RAM) Standard provided instructions: 111 Basic instructions: 77 Single precision floating point instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 (only supported by products with 64 Kbytes of RAM) • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32/32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single-precision (32-bit) floating-point number • Data types and floating-point exceptions in conformance with the IEEE754 standard
	Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks
Memory	Code flash memory	• Capacity: 512 Kbytes, 256 Kbytes, 128 Kbytes • 120 MHz No-wait access • On-board programming: Three types • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	• Capacity: 16 Kbytes • Programming/erasing: 100,000 times
	Unique ID	• 12-byte unique ID for the device
	RAM	• Capacity: 64 Kbytes, 48 Kbytes • 120 MHz No-wait access • SED (single error detection)
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (SCI interface) Boot mode (FINE interface) • Selection of operating mode by register setting Single-chip mode • Endian selectable

Table 1.1 Outline of Specifications (2/9)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), and flash-IF clock (FCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz Peripheral modules of MTU (Internal peripheral bus), GPTW (Internal peripheral bus), HRPWM (Internal peripheral bus), RSPI, RSPIA, RSCI, RI3C, and the ECC function control registers in the CAN FD module run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz MTU (counter reference clocks), GPTW (counter reference clocks), and HRPWM (reference clocks) are synchronized with PCLKC: Up to 120 MHz ADCLK in the S12AD runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Eight types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC rises. • Voltage-monitoring 0 reset: Generated when VCC falls. • Voltage-monitoring 1 reset: Generated when VCC falls. • Voltage-monitoring 2 reset: Generated when VCC falls. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC pin and generates an internal reset or internal interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from two different levels • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from five different levels Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking
Low power consumption	Low power consumption facilities	• Module stop function • Three low power consumption modes Sleep mode, all-module clock stop mode, and software standby mode
Interrupt	Interrupt controller (ICUG)	• Interrupt vectors: 256 • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 7 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors, with 128 having fixed sources. The other 133 sources can be assigned to the remaining 128 vectors as required.

Table 1.1 Outline of Specifications (3/9)

Classification	Module/Function	Description
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCb)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	• I/O ports for the 100-pin LFQFP I/O pins: 82 Input pin: 1 Pull-up resistors: 82 Open-drain outputs: 82 5-V tolerance: 2 Large current output: 15 • I/O ports for the 80-pin LFQFP I/O pins: 62 Input pin: 1 Pull-up resistors: 62 Open-drain outputs: 62 5-V tolerance: 2 Large current output: 14 • I/O ports for the 64-pin LFQFP, 64-pin HWQFN I/O pins: 49 Input pin: 1 Pull-up resistors: 49 Open-drain outputs: 49 5-V tolerance: 2 Large current output: 14 • I/O ports for the 48-pin LFQFP, 48-pin HWQFN I/O pins: 37 Input pin: 1 Pull-up resistors: 37 Open-drain outputs: 37 5-V tolerance: 2 Large current output: 13
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 183 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	8-bit timers (TMRb)	• (8 bits × 2 channels) × 4 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Timers	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
	Multifunction timer pulse unit 3 (MTU3d)	• 9 channels (16 bits × 9 channels) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKC/1, PCLKC/2, PCLKC/4, PCLKC/8, PCLKC/16, PCLKC/32, PCLKC/64, PCLKC/256, PCLKC/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 11 of the signals are available for channels 1, 3, 4, 12 are available for channel 2, and 10 are available for channel 5. • 43 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 45 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion The timing of the generation of requests to start A/D conversion can be monitored by an external pin. • A/D conversion start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • Event linking by the ELC • Internal peripheral bus clock: PCLKA • Counter reference clock: PCLKC • Frequency ratio: PCLKA to PCLKC = 1: N (N = 1 or 2)
	Port output enable 3 (POE3D)	• Control of the high-impedance state of the MTU/GPTW's waveform output pins, and control of switching to the general I/O port pin • 7 pins for input from signal sources: POE0, POE4, POE8, POE9, POE10, POE11, POE12 • Initiation by detection of short-circuited outputs (detection of PWM outputs that have become an active level simultaneously) • Initiation by comparator detection/oscillation stop detection/software • Additional programming of output control target pins is enabled

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	General PWM timer (GPTWa)	• 32 bits × 8 channels (products with 64 Kbytes of RAM) • 16 bits × 8 channels (products with 48 Kbytes of RAM) • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Capable of synchronous start, stop, or clearing of counter for any channel • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 8 ELC events • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 4 external triggers • Output pin disabling function by a dead time error or a short circuit detection among output pins • Capable of generating conversion start triggers for the A/D converters as well as monitoring external pins for a start timing of conversion. • Capable of outputting events, such as compare-match from A to F and overflow/ underflow, to ELC • Capable of using noise filter of input capture • Periodic counting • Internal peripheral bus clock: PCLKA • Counter reference clock: PCLKC • Frequency ratio: PCLKA to PCLKC = 1: N (N = 1 or 2)
	High resolution PWM (HRPWM)	• Capable of generating the PWM waveform that is generated by GPTW0 through GPTW3 with resolution of minimum of 260 ps.
	Port output enable for GPTW (POEG)	• Controlling the output disable for GPTW waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPTW • Initiation by detection of comparator interrupt request • Initiation by detection of oscillation stop or by software

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIk, SCIh)	• 4 channels SCIk: SCI1, SCI5, SCI6 SCIh: SCI12 • SCIk, SCIh Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 7, 8, 9-bit transfer mode Bit rate modulation Double-speed mode Data match detection (SCI12 is not supported) Event linking by the ELC (supported by SCI5 only) RXD input signal select function (supported by SCI5 only) • SCIk Only Data match detection Adjustment of the timing of sampling of the RXD signals • SCIh Only Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	Serial communications interfaces (RSCI)	• 3 channels (RSCI8, RSCI9, RSCI11) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Start-bit detection: Level or edge detection is selectable. • Simple I^2C • Simple SPI • 9-bit transfer mode • Bit rate modulation • Double-speed mode • Event linking by the ELC (only RSCI11) • RXD input signal select function • Supports the serial communications protocol, which contains the start frame and information frame • Supports the LIN format (RSCI9, RSCI11) • Data can be transmitted or received in sequence by the 32-byte FIFO buffers of the transmission and reception unit (only RSCI11) • Manchester encoding is supported. • RSCI has some home bus system (HBS) functionality. • Data match detection • Adjustment of the timing of sampling of the RXD signals
	I^2C bus interface (RIICa)	• 1 channel Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps • Event linking by the ELC

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
Communication function	I3C bus interface (RI3C)	• 1 channel Supports the SDR mode Supports the legacy I^2C message Supports the multi-master • Event linking by the ELC
	CAN FD module (CANFD)	• 1 channel • Compliance with the ISO11898-1:2015 specification (standard frame and extended frame)
	Serial peripheral interface (RSPId)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transmit/receive data can be swapped in byte units • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC
	Serial peripheral interface (RSPIA)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transmit/receive data can be swapped in byte units • Buffered structure The transmission and reception sections have 4-stage and 32-bit-wide FIFO buffers for the sequential transmission and reception of data. • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC • Communications protocol: RSPIA supports the Texas Instruments Synchronous Serial Protocol (TI SSP).

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
12-bit A/D converter (S12ADH) (Products with 64 Kbytes of RAM)		• 12 bits (4 channels × 2 units, 14 channels × 1 unit) • 12-bit resolution • Minimum conversion time 0.9 µs per channel (when ADCLK operates at 60 MHz) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sample-and-hold function channel-dedicated sample-and-hold function (unit 0 × 3 channels, unit 1 × 3 channels) included • Sampling variable Sampling time can be set up for each channel. • Conversion function in order of arbitrarily selected channels (Serial conversion of the same channel cannot be allowed) • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, synchronous trigger (MTU, GPTW, TMR, ELC), external trigger • Prioritization in group scanning can be controlled among group A, B, and C. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function • Detection of analog input disconnection • Event linking by the ELC • Input signal amplification function by the programmable gain amplifier (unit 0 × 3 channels, unit 1 × 3 channels)
12-bit A/D converter (S12ADH) (Products with 48 Kbytes of RAM)		• 12 bits (7 channels × 1 unit, 8 channels × 1 unit) • 12-bit resolution • Minimum conversion time 0.9 µs per channel (when ADCLK operates at 60 MHz) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sample-and-hold function channel-dedicated sample-and-hold function (unit 0 × 3 channels) included • Sampling variable Sampling time can be set up for each channel. • Conversion function in order of arbitrarily selected channels (Serial conversion of the same channel cannot be allowed) • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, synchronous trigger (MTU, GPTW, TMR, ELC), external trigger • Prioritization in group scanning can be controlled among group A, B, and C. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function • Detection of analog input disconnection • Event linking by the ELC
12-bit D/A converter (R12DAb)		• 2 channels • 12-bit resolution • Output voltage: 0 V to AVCC2 • Capable of providing as a reference voltage for comparator • Event linking by the ELC
Comparator C (CMPCa)		• 6 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage is selectable from 4 inputs • Analog input voltage is selectable from 4 inputs • Digital filtering

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Temperature sensor		• 1 channel • Relative precision: ±1.0°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 2).
Arithmetic unit for trigonometric functions (TFUv2)		• Calculation of sine, cosine, arctangent, and hypotenuse Simultaneous calculation of sine and cosine Simultaneous calculation of arctangent and hypotenuse
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$, $X^{32}+X^{28}+X^{27}+X^{26}+X^{25}+X^{23}+X^{22}+X^{20}+X^{19}+X^{18}+X^{14}+X^{13}+X^{11}+X^{10}+X^9+X^8+X^6+1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOCA)	• This handles the comparison, addition, subtraction, comparison in terms of which is larger or smaller, or window comparison of 32-bit values.
Encryption functions	Trusted Secure IP (TSIP-Lite)	• Access management circuit • Encryption engine 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Prevention from illicit copying of a key
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = 2.7 to 5.5V AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V (VCC ≤ AVCC0 = AVCC1 = AVCC2) VSS = AVSS0 = AVSS1 = AVSS2 = 0V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C
Package		100-pin LFQFP 0.5 mm pitch 80-pin LFQFP 0.5 mm pitch 64-pin LFQFP 0.5 mm pitch 64-pin HWQFN 0.5 mm pitch 48-pin LFQFP 0.5 mm pitch 48-pin HWQFN 0.5 mm pitch
Debugging interfaces		• JTAG and One-line FINE interfaces

Table 1.2 Comparison of Functions for Different Packages (1/2)

Module/Functions		RX26T Group					
		Products with 64 Kbytes of RAM				Products with 48 Kbytes of RAM	
		100 Pins	80 Pins	64 Pins	48 Pins	64 Pins	48 Pins
CPU	Register Bank Save Function	Available				Not available	
Code Flash Memory	Code flash memory capacity	128 Kbytes/256 Kbytes/512 Kbytes				128 Kbytes/256 Kbytes	
	Dual bank function	Available*1				Not available	
	BGO function	Available					
Data Flash Memory		16 Kbytes					
RAM		64 Kbytes				48 Kbytes	
External interrupts	NMI	Available					
	IRQ	16 channels	13 channels	12 channels	10 channels	12 channels	10 channels
DMA	DMA controller	Available					
	Data transfer controller	Available					
Timers	Multifunction timer pulse unit 3	9 channels (Ch. 0 to 7, Ch. 9)					
	General PWM timer	32 bits × 8 channels				16 bits × 8 channels	
	High resolution PWM	4 channels				Not available	
	Port output enable 3	Available					
	Port Output Enable for GPTW	Available					
	8-bit timer	2 channels × 4 units					
	Compare match timer	2 channels × 2 units					
	Compare match timer W	1 channel × 2 units					
	Watchdog timer	Available					
	Independent watchdog timer	Available					
Communication functions	Serial communications interfaces (SCIk)	Ch. 1, 5, and 6					
	Serial communications interfaces (SCIh)	Ch. 12					
	Serial communications interfaces (RSCI)	Ch. 8, 9, and 11				Not available	
	I2C bus interfaces (RIIC)	1 channel					
	I3C bus interfaces (RI3C)	1 channel				Not available	
	Serial peripheral interface (RSPI)	Ch. 0					
	Serial peripheral interface (RSPIA)	Ch. 0				Not available	
	CAN FD module (CANFD)	1 channel					
12-bit A/D Converter		Unit 0: 4 channels Unit 1: 4 channels Unit 2: 14 channels	Unit 0: 4 channels Unit 1: 4 channels Unit 2: 11 channels	Unit 0: 4 channels Unit 1: 4 channels Unit 2: 7 channels	Unit 0: 4 channels Unit 1: 1 channels Unit 2: 5 channels	Unit 0: 7 channels Unit 2: 8 channels	Unit 0: 5 channels Unit 2: 5 channels
	3 channels simultaneous sampling function	Available (unit 0, 1)			Available (unit 0)		
	Programmable gain amplifier	6 channels			4 channels	Not available	
Comparator C		6 channels			5 channels	4 channels	
D/A converter		2 channels					
Temperature sensor		1 channel					

Table 1.2 Comparison of Functions for Different Packages (2/2)

Module/Functions	RX26T Group					
	Products with 64 Kbytes of RAM				Products with 48 Kbytes of RAM	
	100 Pins	80 Pins	64 Pins	48 Pins	64 Pins	48 Pins
Arithmetic unit for trigonometric functions (TFU)	Available					
CRC calculator (CRC)	Available					
Data operation circuit (DOC)	Available					
Clock frequency accuracy measurement circuit (CAC)	Available					
Trusted Secure IP (TSIP-Lite)	Available/Not available				Not available	
Event link controller (ELC)	Available					
Packages	100-pin LFQFP	80-pin LFQFP	64-pin LFQFP 64-pin HWQFN	48-pin LFQFP 48-pin HWQFN	64-pin LFQFP	48-pin LFQFP

Note 1. The products with 512 Kbytes of the code flash memory only support this function.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/3)

Group	Part No.	Package	ROM Capacity	RAM Capacity	CANFD	TSIP-Lite	Operating temperature
RX26T (D-version)	R5F526T9ADFP	PLQP0100KB-B	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9BDFP	PLQP0100KB-B	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBADFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TBBDFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBCDFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBDDFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526TFADFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TFBDFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TFCDFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TFDDFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526T9ADFN	PLQP0080KB-B	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9BDFN	PLQP0080KB-B	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBADFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TBBDFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBCDFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBDDFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526TFADFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TFBDFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TFCDFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TFDDFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526T8ADFM	PLQP0064KB-C	128 Kbytes	48 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9ADFM	PLQP0064KB-C	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9BDFM	PLQP0064KB-C	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TAADFM	PLQP0064KB-C	256 Kbytes	48 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TACDFM	PLQP0064KB-C	256 Kbytes	48 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBADFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TBBDFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBCDFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBDDFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526TFADFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TFBDFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TFCDFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TFDDFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526T9ADND	PWQN0064KF-A	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9BDND	PWQN0064KF-A	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBADND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TBBDND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBCDND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBDDND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526TFADND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TFBDND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TFCDND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TFDDND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available	Available	-40 to 85°C

Table 1.3 List of Products (2/3)

Group	Part No.	Package	ROM Capacity	RAM Capacity	CANFD	TSIP-Lite	Operating temperature
RX26T (D-version)	R5F526T8ADFL	PLQP0048KB-B	128 Kbytes	48 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9ADFL	PLQP0048KB-B	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9BDFL	PLQP0048KB-B	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TAADFL	PLQP0048KB-B	256 Kbytes	48 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TACDFL	PLQP0048KB-B	256 Kbytes	48 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBADFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TBBDFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBCDFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBDDFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526TFADFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TFBDFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TFCDFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TFDDFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526T9ADNE	PWQN0048KC-A	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526T9BDNE	PWQN0048KC-A	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBADNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TBBDNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TBCDNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TBDDNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
	R5F526TFADNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 85°C
	R5F526TFBDNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 85°C
	R5F526TFCDNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available	Not available	-40 to 85°C
	R5F526TFDDNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available	Available	-40 to 85°C
RX26T (G-version)	R5F526T9AGFP	PLQP0100KB-B	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9BGFP	PLQP0100KB-B	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBAGFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TBBGFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBCGFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBDGFP	PLQP0100KB-B	256 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526TFAGFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TFBGFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TFCGFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TFDGFP	PLQP0100KB-B	512 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526T9AGFN	PLQP0080KB-B	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9BGFN	PLQP0080KB-B	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBAGFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TBBGFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBCGFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBDGFN	PLQP0080KB-B	256 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526TFAGFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TFBGFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TFCGFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TFDGFN	PLQP0080KB-B	512 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526T8AGFM	PLQP0064KB-C	128 Kbytes	48 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9AGFM	PLQP0064KB-C	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9BGFM	PLQP0064KB-C	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TAAGFM	PLQP0064KB-C	256 Kbytes	48 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TACGFM	PLQP0064KB-C	256 Kbytes	48 Kbytes	Available	Not available	-40 to 105°C

Table 1.3 List of Products (3/3)

Group	Part No.	Package	ROM Capacity	RAM Capacity	CANFD	TSIP-Lite	Operating temperature
RX26T (G-version)	R5F526TBAGFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TBBGFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBCGFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBDGFM	PLQP0064KB-C	256 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526TFAGFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TFBGFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TFCGFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TFDGFM	PLQP0064KB-C	512 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526T9AGND	PWQN0064KF-A	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9BGND	PWQN0064KF-A	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBAGND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TBBGND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBCGND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBDGND	PWQN0064KF-A	256 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526TFAGND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TFBGND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TFCGND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TFDGND	PWQN0064KF-A	512 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526T8AGFL	PLQP0048KB-B	128 Kbytes	48 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9AGFL	PLQP0048KB-B	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9BGFL	PLQP0048KB-B	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TAAGFL	PLQP0048KB-B	256 Kbytes	48 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TACGFL	PLQP0048KB-B	256 Kbytes	48 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBAGFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TBBGFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBCGFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBDGFL	PLQP0048KB-B	256 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526TFAGFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TFBGFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TFCGFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TFDGFL	PLQP0048KB-B	512 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526T9AGNE	PWQN0048KC-A	128 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526T9BGNE	PWQN0048KC-A	128 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBAGNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TBBGNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TBCGNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TBDGNE	PWQN0048KC-A	256 Kbytes	64 Kbytes	Available	Available	-40 to 105°C
	R5F526TFAGNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available*1	Not available	-40 to 105°C
	R5F526TFBGNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available*1	Available	-40 to 105°C
	R5F526TFCGNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available	Not available	-40 to 105°C
	R5F526TFDGNE	PWQN0048KC-A	512 Kbytes	64 Kbytes	Available	Available	-40 to 105°C

Note 1. Products with this part number support only CAN 2.0 protocol.

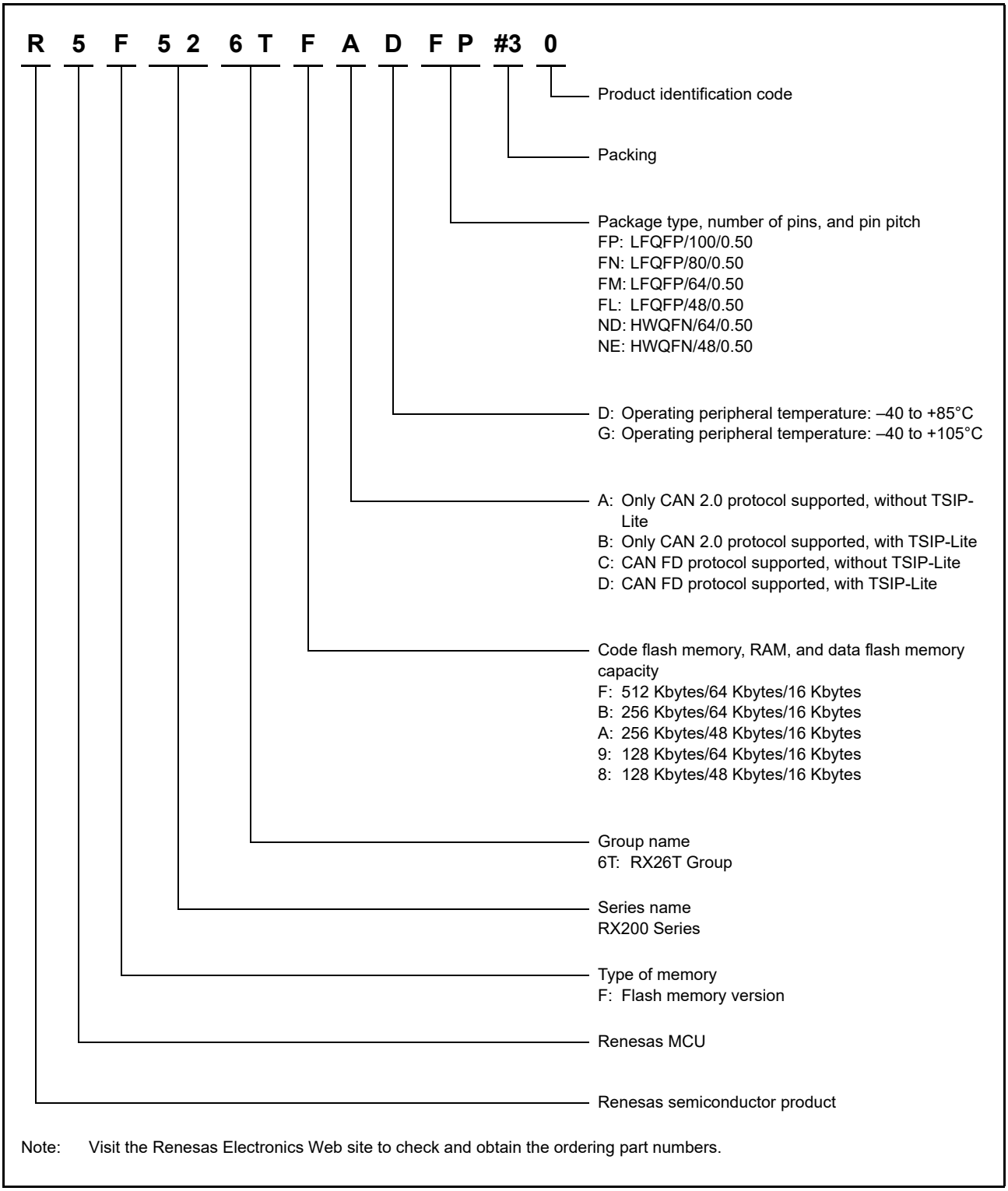


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 and Figure 1.3 show block diagrams.

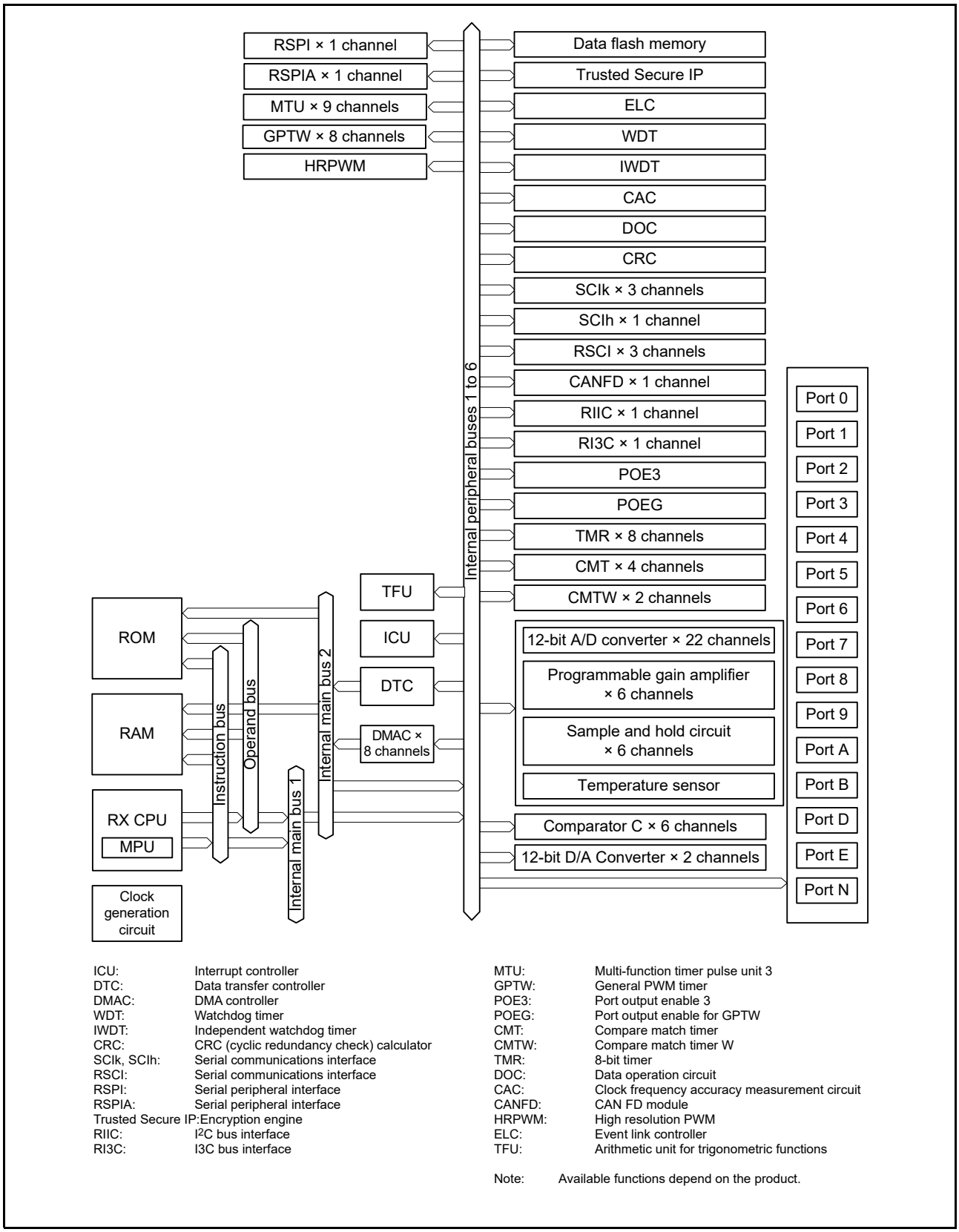


Figure 1.2 Block Diagram (Products with 64 Kbytes of RAM)

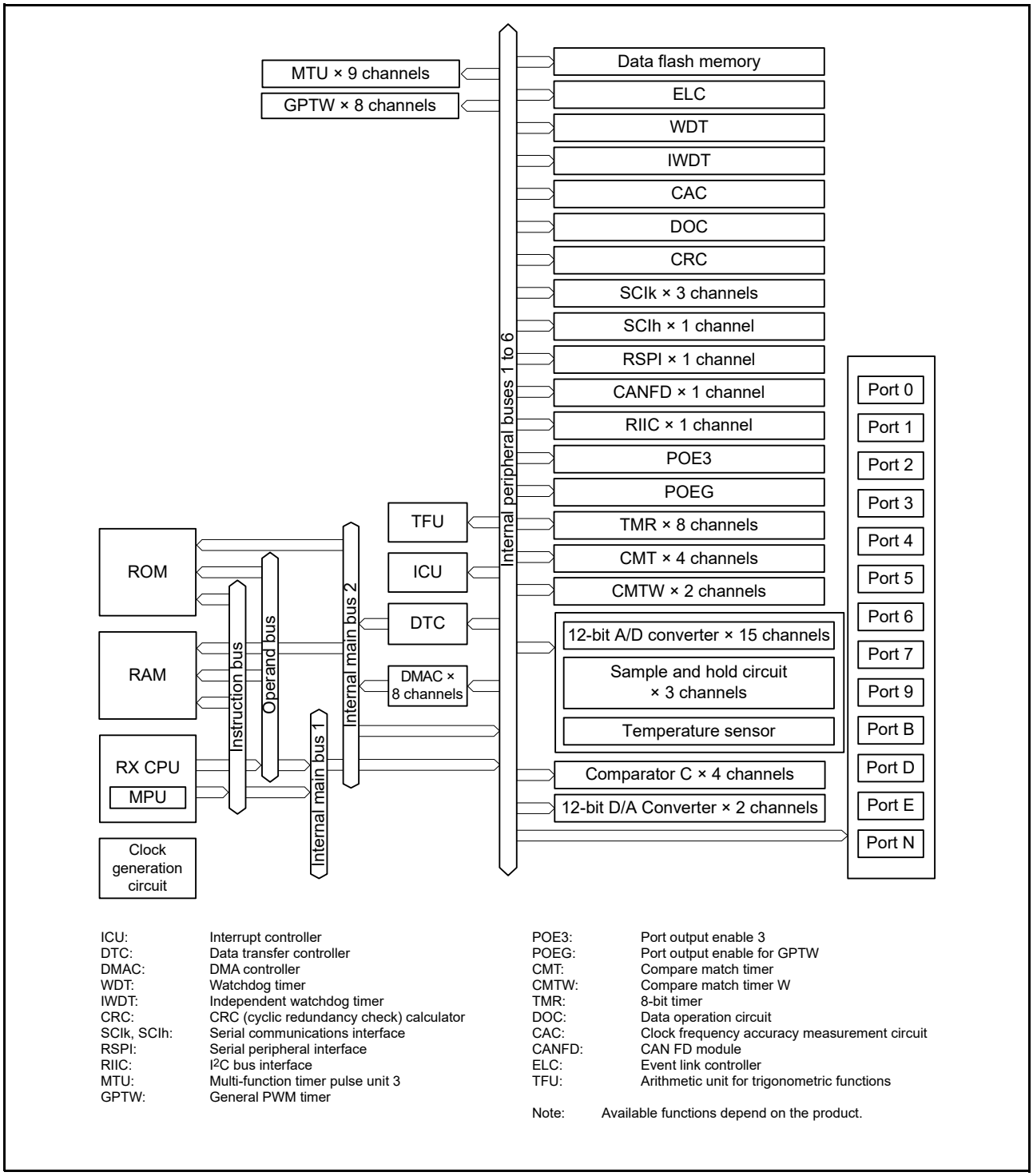


Figure 1.3 Block Diagram (Products with 48 Kbytes of RAM)

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/5)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.47-μF smoothing capacitor used to stabilize the internal power supply. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	FINE interface pin.
	TRST#	Input	Pins for the on-chip emulator. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC0A#, MTIOC0B#, MTIOC0C#, MTIOC0D#	I/O	The TGRA0 to TGRD0 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC1A#, MTIOC1B#	I/O	The TGRA1 and TGRB1 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC2A#, MTIOC2B#	I/O	The TGRA2 and TGRB2 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC3A#, MTIOC3B#, MTIOC3C#, MTIOC3D#	I/O	The TGRA3 to TGRD3 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIOC4A#, MTIOC4B#, MTIOC4C#, MTIOC4D#	I/O	The TGRA4 to TGRD4 input capture inverted input/output compare inverted output/PWM inverted output pins.

Table 1.4 Pin Functions (2/5)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins
	MTIC5U#, MTIC5V#, MTIC5W#	Input	The TGRU5, TGRV5, and TGRW5 input capture inverted input/ external pulse inverted input pins.
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC6A#, MTIOC6B#, MTIOC6C#, MTIOC6D#	I/O	The TGRA6 to TGRD6 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC7A#, MTIOC7B#, MTIOC7C#, MTIOC7D#	I/O	The TGRA7 to TGRD7 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D	I/O	The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins
	MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D#	I/O	The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D conversion start request frame synchronization signal output pins.
General PWM timer	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC7A, GTIOC0B to GTIOC7B	I/O	Input capture input/output compare output/PWM output pins
	GTIOC0A# to GTIOC7A#, GTIOC0B# to GTIOC7B#	I/O	Input capture inverted input/output compare inverted output/ PWM inverted output pins
	GTCPPO0, GTCPPO4	Output	Synchronized PWM output
	GTIU, GTIV, GTIW	Input	Hall sensor input pins
	GTOUUP	Output	A three-phase PWM output for controlling a brushless DC motor (positive U-phase)
	GTOULO	Output	A three-phase PWM output for controlling a brushless DC motor (negative U-phase)
	GTOVUP	Output	A three-phase PWM output for controlling a brushless DC motor (positive V-phase)
	GTOVLO	Output	A three-phase PWM output for controlling a brushless DC motor (negative V-phase)
	GTOWUP	Output	A three-phase PWM output for controlling a brushless DC motor (positive W-phase)
	GTOWLO	Output	A three-phase PWM output for controlling a brushless DC motor (negative W-phase)
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer	TMO0 to TMO7	Output	Compare match output pins.
	TMCI0 to TMCI7	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI7	Input	Counter reset input pins.
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW
Port output enable 3	POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#	Input	Input pins for request signals to switch the MTU and GPTW pins between the high impedance state

Table 1.4 Pin Functions (3/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIk)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock
	RXD1, RXD5, RXD6	Input	Input pins for received data
	TXD1, TXD5, TXD6	Output	Output pins for transmitted data
	CTS1#, CTS5#, CTS6#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock
	SMISO1, SMISO5, SMISO6	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#	Input	Chip-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (RSCI)	• Asynchronous mode/clock synchronous mode		
	SCK008, SCK009, SCK011	I/O	Input/output pins for the clock
	RXD008, RXD009, RXD011	Input	Input pins for received data
	TXD008, TXD009, TXD011	Output	Output pins for transmitted data
	CTS008#, CTS009#, CTS011#	Input	Input pins for controlling the start of transmission and reception
	RTS008#, RTS009#, RTS011#	Output	Output pins for controlling the start of transmission and reception
	DE008, DE009, DE011	Output	DriveEnable output pins
	• Simple I^2C mode		
	SSCL008, SSCL009, SSCL011	I/O	Input/output pins for the I^2C clock
	SSDA008, SSDA009, SSDA011	I/O	Input/output pins for the I^2C data

Table 1.4 Pin Functions (4/5)

Classifications	Pin Name	I/O	Description
Serial communications interface (RSCI)	• Simple SPI mode		
	SCK008, SCK009, SCK011	I/O	Input/output pins for the clock
	SMISO008, SMISO009, SMISO011	I/O	Input/output pins for slave transmission of data
	SMOSI008, SMOSI009, SMOSI011	I/O	Input/output pins for master transmission of data
	SS008#, SS009#, SS011#	Input	Chip-select input pins
	• HBS support mode		
	RXD008, RXD009, RXD011	Input	Input pins for received data
	TXDA008, TXDA009, TXDA011	Output	Output pins for transmitted data
	TXDB008, TXDB009, TXDB011		
I^2C bus interface	SCL0	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.
I3C bus interface	SCL00	I/O	Input/output pin for I3C bus interface clocks.
	SDA00	I/O	Input/output pin for I3C bus interface data.
CAN FD module	CRX0	Input	Input pins
	CTX0	Output	Output pins
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
Serial peripheral interface (RSPIA)	RSPCK0	I/O	Input/output pin for the RSPIA clock.
	MOSI0	I/O	Input/output pin for transmitting data from the RSPIA master.
	MISO0	I/O	Input/output pin for transmitting data from the RSPIA slave.
	SSL00	I/O	Input/output pin to select the slave for the RSPIA.
	SSL01 to SSL03	Output	Output pins to select the slave for the RSPIA.
12-bit A/D converter	AN000 to AN006, AN100 to AN103, AN200 to AN211, AN216, AN217	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADST0, ADST1, ADST2	Output	Output pins for A/D conversion status.
	ADTRG0#, ADTRG1#, ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator C	COMP0 to COMP5	Output	Comparator detection result output pins.
	CVREFC0, CVREFC1	Input	Analog reference voltage supply pins for comparator C.
	CMPCnm	Input	Analog input pin for CMPCnm (n = 0 to 5, m = 0 to 3)

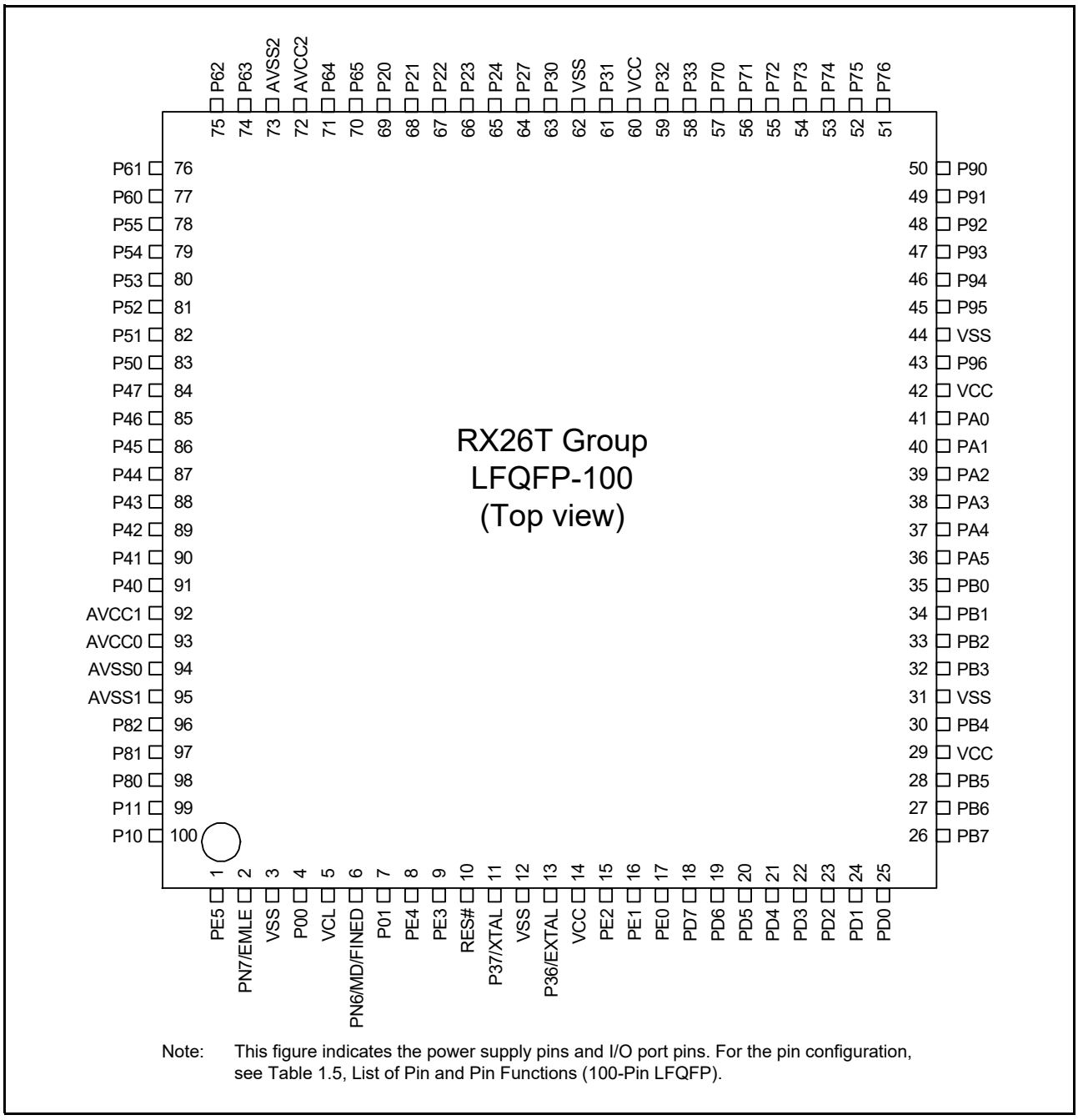
Table 1.4 Pin Functions (5/5)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1 or AVCC2 when 12-bit A/D converter unit 0 is not used.
	AVSS0	Input	Analog ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used.
	AVCC1	Input	Analog voltage supply pin for 12-bit A/D converter unit 1. Connect this pin to AVCC0 when not using the 12-bit A/D converter 1 but using the 12-bit A/D converter 0. Connect this pin to AVCC2 when not using the 12-bit A/D converter 0 and the 12-bit A/D converter 1.
	AVSS1	Input	Analog ground pin for 12-bit A/D converter unit 1. Connect this pin to AVSS0 when not using the 12-bit A/D converter 1 but using the 12-bit A/D converter 0. Connect this pin to AVSS2 when not using the 12-bit A/D converter 0 and the 12-bit A/D converter 1.
	AVCC2	Input	Analog voltage supply pin for the 12-bit A/D converter unit 2, reference voltage supply pin for the 12-bit D/A converter, analog voltage supply pin for the comparator C, and analog voltage supply pin for the temperature sensor. Connect this pin to either of AVCC0 or AVCC1 when not using the 12-bit A/D converter unit 2, 12-bit D/A converter, comparator C, and temperature sensor.
	AVSS2	Input	Analog ground pin for the 12-bit A/D converter unit 2, reference ground pin for the D/A converter, analog ground pin for the comparator C, and analog ground pin for the temperature sensor. Connect this pin to either of AVSS0 or AVSS1 when not using the 12-bit A/D converter unit 2, 12-bit D/A converter, comparator C, and temperature sensor.
I/O ports	P00, P01	I/O	General-purpose input/output pins
	P10, P11	I/O	General-purpose input/output pins
	P20 to P24, P27	I/O	General-purpose input/output pins
	P30 to P33, P36, P37	I/O	General-purpose input/output pins
	P40 to P47	I/O	General-purpose input/output pins
	P50 to P55	I/O	General-purpose input/output pins
	P60 to P65	I/O	General-purpose input/output pins
	P70 to P76	I/O	General-purpose input/output pins
	P80 to P82	I/O	General-purpose input/output pins
	P90 to P96	I/O	General-purpose input/output pins
	PA0 to PA5	I/O	General-purpose input/output pins
	PB0 to PB7	I/O	General-purpose input/output pins
	PD0 to PD7	I/O	General-purpose input/output pins
	PE0 to PE5	I/O	General-purpose input/output pins (PE2: input pin)
	PN6*1, PN7*2	I/O	General-purpose input/output pins

Note: When not using any of the A/D converter, D/A converter, comparator C and temperature sensor, connect the AVCC0, AVCC1 and AVCC2 pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.
Note 1. This pin functions as MD after release from the reset state, and the pull-up resistor connected to the MD pin is enabled.
Note 2. This pin functions as EMLE after release from the reset state, and the pull-down resistor connected to the EMLE pin is enabled.

1.5 Pin Assignments

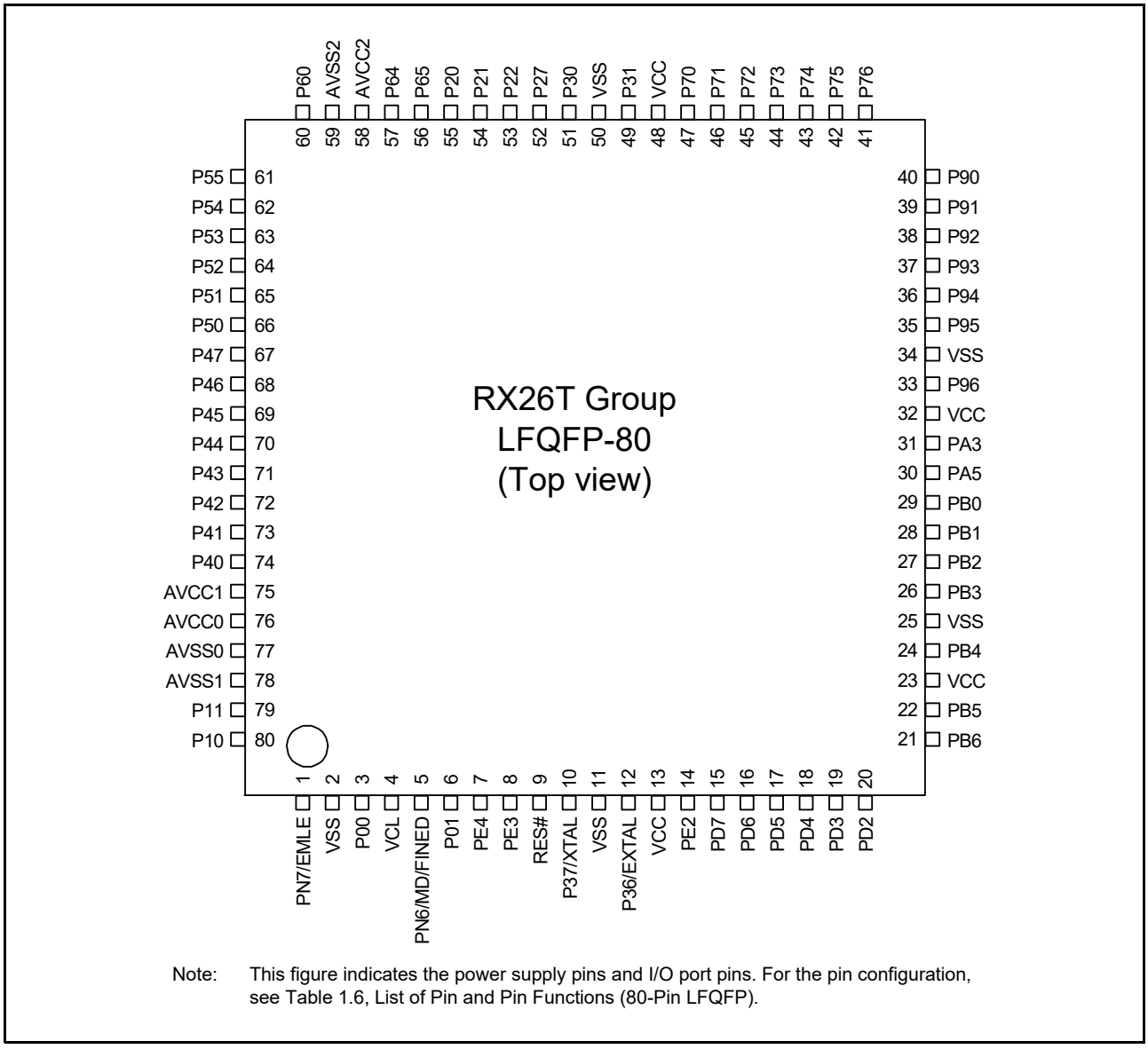
1.5.1 100-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.4 Pin Assignment (100-pin LFQFP)

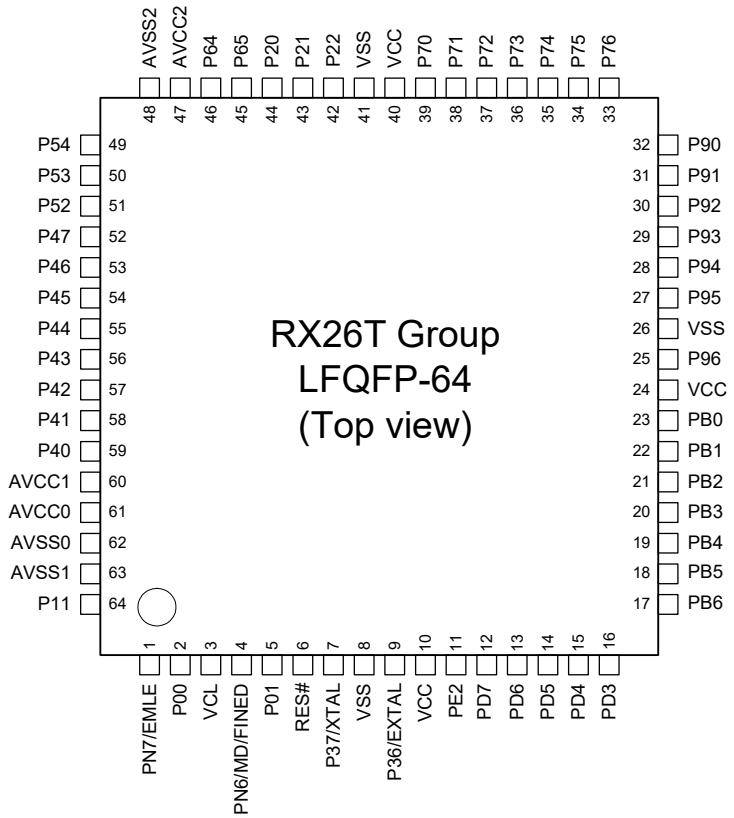
1.5.2 80-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (80-Pin LFQFP).

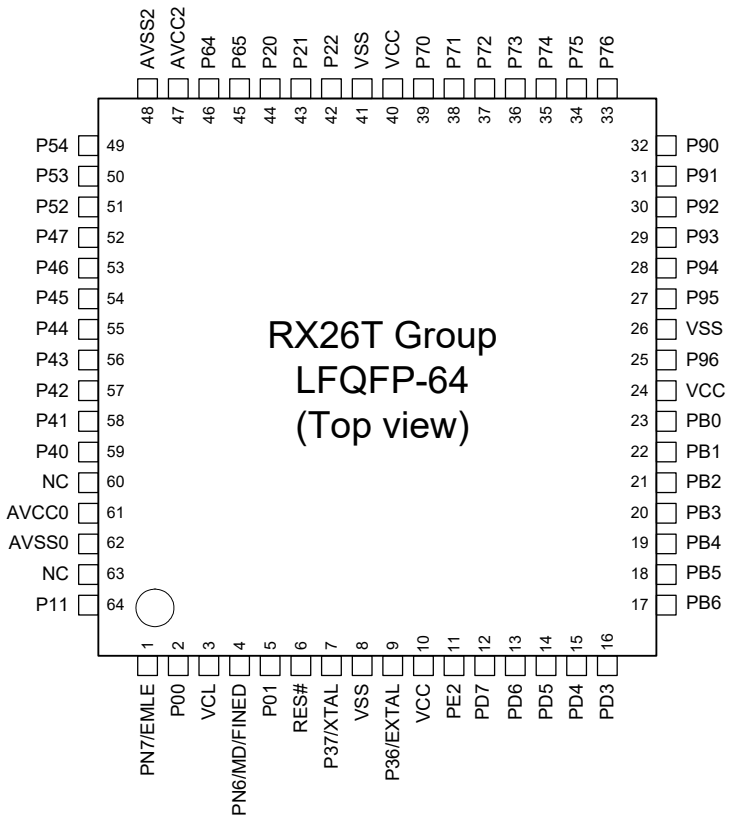
Figure 1.5 Pin Assignment (80-pin LFQFP)

1.5.3 64-Pin LFQFP and 64-Pin HWQFN



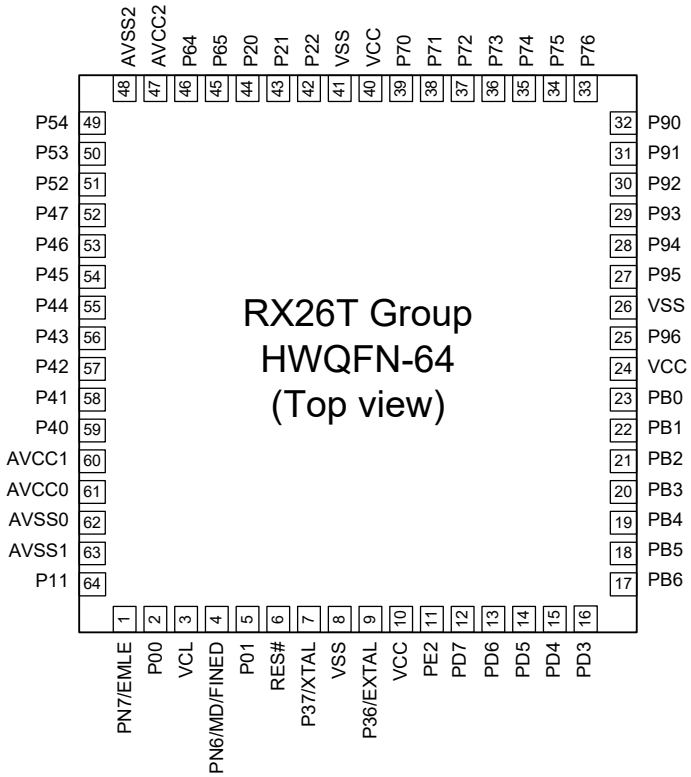
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (64-Pin LFQFP, 64-Pin HWQFN) (Products with 64 Kbytes of RAM).

Figure 1.6 Pin Assignment (64-pin LFQFP) (Products with 64 Kbytes of RAM)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (64-Pin LFQFP) (Products with 48 Kbytes of RAM).

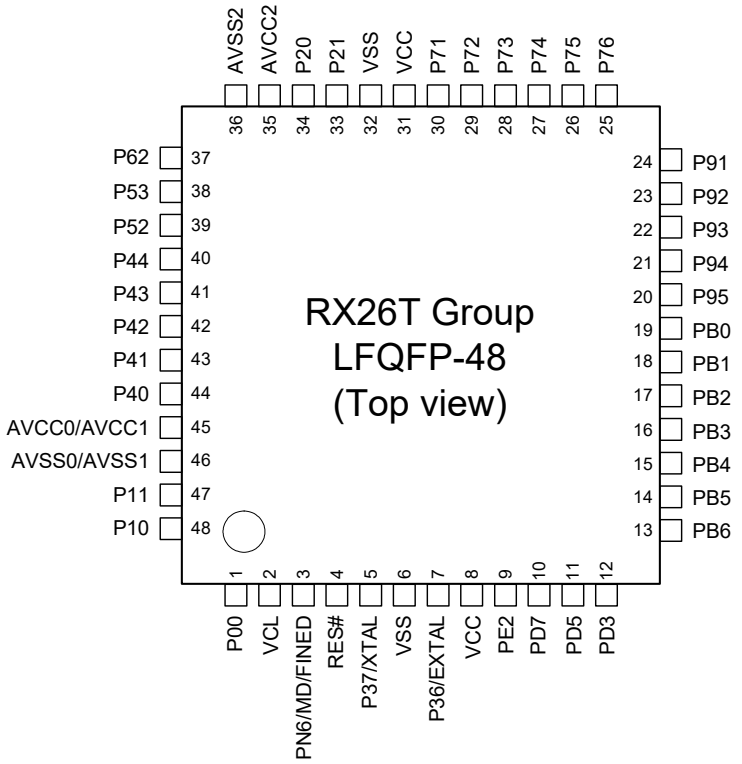
Figure 1.7 Pin Assignment (64-pin LFQFP) (Products with 48 Kbytes of RAM)



Note: We recommend connecting the exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (64-Pin LFQFP, 64-Pin HWQFN) (Products with 64 Kbytes of RAM).

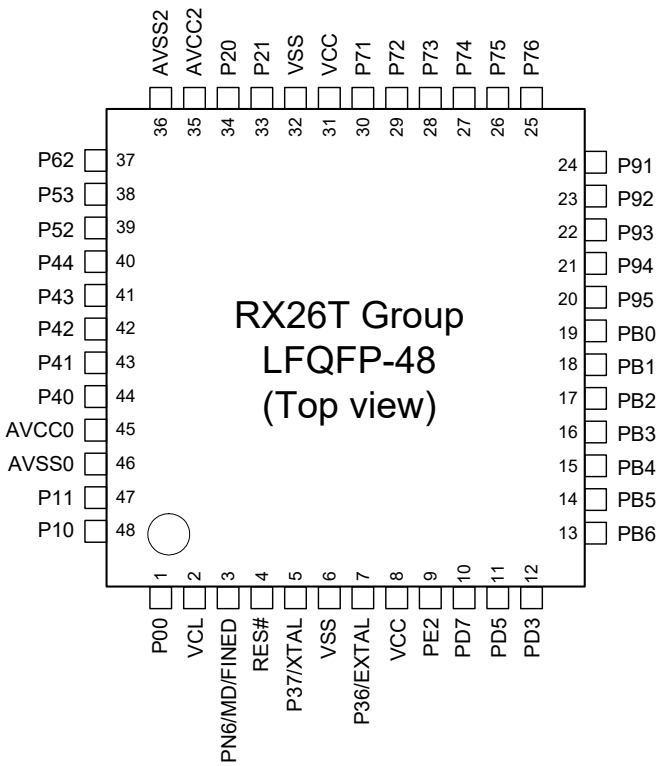
Figure 1.8 Pin Assignment (64-pin HWQFN)

1.5.4 48-Pin LFQFP and 48-Pin HWQFN



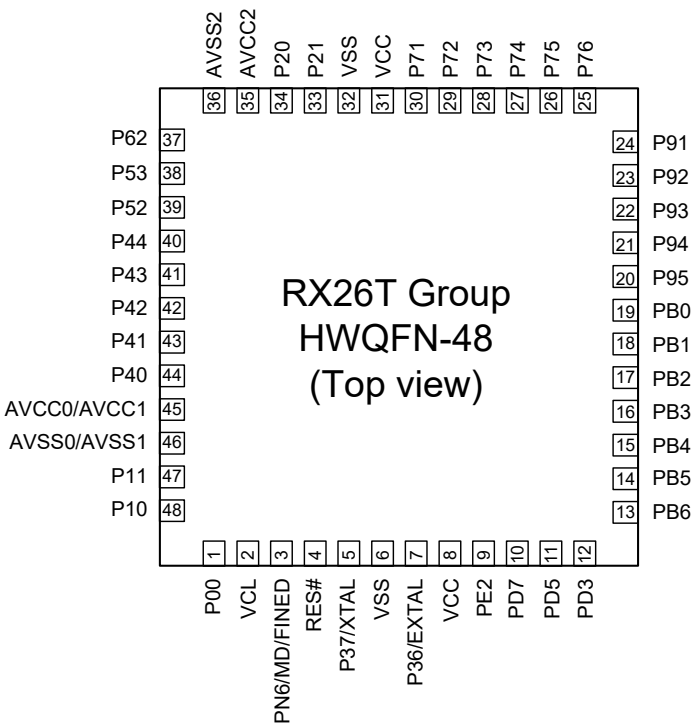
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (Products with 64 Kbytes of RAM).

Figure 1.9 Pin Assignment (48-pin LFQFP) (Products with 64 Kbytes of RAM)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pin and Pin Functions (48-Pin LFQFP) (Products with 48 Kbytes of RAM).

Figure 1.10 Pin Assignment (48-pin LFQFP) (Products with 48 Kbytes of RAM)



Note: We recommend connecting the exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (Products with 64 Kbytes of RAM).

Figure 1.11 Pin Assignment (48-pin HWQFN)

1.6 List of Pin and Pin Functions

1.6.1 100-Pin LFQFP

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (1/6)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
1		PE5	MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/ GTIOC3A#/GTETRGD	SCK009/CTS009#/ RTS009#/SS009#/TXDB009	IRQ0	ADST0
2	EMLE	PN7	MTIOC9D/MTIOC9D#		IRQ5	ADST0
3	VSS					
4		P00	MTIOC9A/MTIOC9A#/ CACREF/GTIU/TIC3	RXD12/SMISO12/SSCL12/ RXDX12/RXD009/ SMISO009/SSCL009	IRQ2	ADST1/ COMP0
5	VCL					
6	MD/FINED	PN6				
7		P01	MTIOC9C/MTIOC9C#/ POE12#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTIW	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/ TXDA009/SMOSI009/ SSDA009	IRQ4	ADST2/ COMP1
8		PE4	MTCLKC/MTCLKC#/ POE10#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD	SCK009/TXDB009	IRQ1	
9		PE3	MTCLKD/MTCLKD#/ POE11#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD	CTS009#/RTS009#/SS009#/ DE009	IRQ2	
10	RES#					
11	XTAL	P37		RXD5/SMISO5/SSCL5		
12	VSS					
13	EXTAL	P36		TXD5/SMOSI5/SSDA5		
14	VCC					
15		PE2	POE10#		NMI/IRQ0	
16		PE1	MTIOC9D/MTIOC9D#/TMO5	CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/ SSLA3/SSL03	IRQ15	
17		PE0	MTIOC9B/MTIOC9B#/ TMCI1/TMCI5/GTIV	RXD5/SMISO5/SSCL5/ SSLA2/SSL02/CRX0	IRQ7	
18	TRST#	PD7	MTIOC9A/MTIOC9A#/ TMRI1/TMRI5/GTIOC0A/ GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU	TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/ SMOSI008/SSDA008/ TXDB009/SSLA1/SSL01/ CTX0	IRQ8	
19	TMS	PD6	MTIOC9C/MTIOC9C#/ TMO1/GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ GTIW	CTS1#/RTS1#/SS1#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/DE011/ SSLA0/SSL00	IRQ5	ADST0
20	TDI	PD5	TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/ GTIOC7A	RXD1/SMISO1/SSCL1/ RXD011/SMISO011/ SSCL011/SSL00	IRQ6	

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (2/6)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
21	TCK	PD4	TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#	SCK1/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02	IRQ2	
22	TDO	PD3	TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B	TXD1/SMOSI1/SSDA1/ TXD011/TXDA011/ SMOSI011/SSDA011/MOSI0		
23		PD2	TMCI1/TMO4/GTIOC2B/ GTIOC0A/GTIOC2B#/ GTIOC0A#	SCK5/SCK008/TXDB008/ MOSIA/MOSI0		
24		PD1	TMO2/GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#	RXD008/SMISO008/ SSCL008/MISOA/MISO0		
25		PD0	TMO6/GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#	TXD008/TXDA008/ SMOSI008/SSDA008/ RSPCKA/RSPCK0		
26		PB7	GTIOC1B/GTIOC1B#	SCK5/SCK12/SCK011/ TXDB011/SSL03		
27		PB6	GTIOC2A/GTIOC3A/ GTIOC2A#/GTIOC3A#/ TOC0	RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/ RXDX12/RXD011/ SMISO011/SSCL011/MISO0/ CRX0	IRQ2	
28		PB5	GTIOC2B/GTIOC3B/ GTIOC2B#/GTIOC3B#/TIC0	TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD011/ TXDA011/SMOSI011/ SSDA011/RSPCK0/CTX0		
29	VCC					
30		PB4	POE8#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	CTS5#/RTS5#/SS5#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/SCK011/ TXDB011/MISOA/SSL01/ CRX0	IRQ3	
31	VSS					
32		PB3	MTIOC0A/MTIOC0A#/ CACREF/GTIU/TOC1	SCK6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ CTS009#/RTS009#/SS009#/ DE009/RSPCKA/CTX0	IRQ9	
33		PB2	MTIOC0B/MTIOC0B#/ TMRI0/GTADSM0/ GTIOC7A/GTIOC7A#/GTIV/ TIC1	TXD6/SMOSI6/SSDA6/ SDA0/SDA00		ADSM0
34		PB1	MTIOC0C/MTIOC0C#/ TMCI0/GTADSM1/ GTIOC7B/GTIOC7B#/GTIW/ TOC2	RXD6/SMISO6/SSCL6/ SCL0/SCL00	IRQ4	ADSM1
35		PB0	MTIOC0D/MTIOC0D#/ TMO0/TIC2	TXD6/SMOSI6/SSDA6/ TXD008/TXDA008/ SMOSI008/SSDA008/ CTS011#/RTS011#/SS011#/ DE011/MOSIA/MOSI0	IRQ8	ADTRG2#
36		PA5	MTIOC1A/MTIOC1A#/ TMCI3	RXD6/SMISO6/SSCL6/ RXD008/SMISO008/ SSCL008/MISOA/MISO0	IRQ1	ADTRG1#

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (3/6)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
37		PA4	MTIOC1B/MTIOC1B#/ TMCI7	SCK6/TXD008/TXDA008/ SMOSI008/SSDA008/ RSPCKA/RSPCK0		ADTRG0#
38		PA3	MTIOC2A/MTIOC2A#/ TMRI7/GTADSM0	TXD009/TXDA009/ SMOSI009/SSDA009/ SCK008/TXDB008/SSLA0/ SSL00		
39		PA2	MTIOC2B/MTIOC2B#/ TMO7/GTADSM1	CTS6#/RTS6#/SS6#/ RXD009/SMISO009/ SSCL009/SSLA1/SSL01		
40		PA1	MTIOC6A/MTIOC6A#/ TMO4/GTCPPO4	TXD009/TXDA009/ SMOSI009/SSDA009/ RXD011/SMISO011/ SSCL011/SSLA2/SSL02/ CRX0	IRQ14	ADTRG0#
41		PA0	MTIOC6C/MTIOC6C#/TMO2	SCK009/TXD011/TXDA011/ SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/ CTX0		
42	VCC					
43		P96	POE4#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO4	CTS008#/RTS008#/SS008#/ DE008/SSL03/RSPCK0	IRQ4	
44	VSS					
45		P95	MTIOC6B/MTIOC1A/ MTIOC6B#/MTIOC1A#/ TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/ GTOUUP	RXD6/SMISO6/SSCL6/ RXD008/SMISO008/ SSCL008/MISOA/SSL02/ MISO0	IRQ1	ADTRG1#
46		P94	MTIOC7A/MTIOC2A/ MTIOC7A#/MTIOC2A#/ TMRI7/GTIOC5A/ GTADSM0/GTIOC5A#/ GTOVUP	TXD009/TXDA009/ SMOSI009/SSDA009/ SCK008/TXDB008/SSLA0/ SSL00		
47		P93	MTIOC7B/MTIOC6A/ MTIOC7B#/MTIOC6A#/ TMO4/GTIOC6A/GTIOC6A#/ GTOWUP	TXD009/TXDA009/ SMOSI009/SSDA009/ RXD011/SMISO011/ SSCL011/SSLA2/SSL02/ MOSI0/CRX0	IRQ14	ADTRG0#
48		P92	MTIOC6D/MTIOC6C/ MTIOC6D#/MTIOC6C#/ TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/ GTOULO	SCK009/TXD011/TXDA011/ SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/ MISO0/CTX0		
49		P91	MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC5B#/ GTOVLO	RXD5/SMISO5/SSCL5/ RSPCK0		
50		P90	MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC6B#/ GTOWLO	TXD5/SMOSI5/SSDA5/ SSL01		
51		P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#/ GTOWLO	SSL03		

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (4/6)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
52		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#/ GTOVLO	SSL02		
53		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTOULO	SSL01		
54		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#/ GTOWUP	SSL00		
55		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#/ GTOVUP	MOSI0		
56		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#/ GTOUUP	MISO0		
57		P70	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/ RSPCK0	IRQ5	
58		P33	MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/ TMO0/GTIOC3B/GTIOC7B/ GTIOC3B#/GTIOC7B#/ GTCPPO0	SSLA3/SSL03	IRQ13	
59		P32	MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/ TMO6/GTIOC3A/GTIOC7A/ GTIOC3A#/GTIOC7A#	SSLA2/SSL02	IRQ12	
60	VCC					
61		P31	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6/GTIU	SSLA1/SSL01	IRQ6	
62	VSS					
63		P30	MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMCI6/GTIV	SCK008/CTS008#/ RTS008#/SS008#/DE008/ SSLA0/SSL00	IRQ7	COMP3
64		P27	MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/ TMO2/TMO6/POE9#	RSPCKA/RSPCK0	IRQ15	
65		P24	MTIC5U/MTIC5U#/TMCI2/ TMO6	CTS008#/RTS008#/SS008#/ SCK008/DE008/RSPCKA/ RSPCK0	IRQ4	COMP0
66		P23	MTIC5V/MTIC5V#/TMO2/ CACREF	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD008/ TXDA008/SMOSI008/ SSDA008/MOSIA/MOSI0/ CTX0	IRQ11	COMP1

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (5/6)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
67		P22	MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ TMRI2/TMO4/MTIOC9B/ GTIV	RXD12/SMISO12/SSCL12/ RXDX12/RXD008/ SMISO008/SSCL008/ SCK008/TXDB008/MISOA/ MISO0/CRX0	IRQ10	ADTRG2#/ COMP2
68		P21	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4/TMO6/GTIU	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD008/ TXDA008/SMOSI008/ SSDA008/MOSIA/MOSI0	IRQ6	AN217/ ADTRG1#/ COMP5
69		P20	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4/TMO2/GTIW	CTS008#/RTS008#/SS008#/ RXD008/SMISO008/ SSCL008/DE008/RSPCKA/ RSPCK0	IRQ7	AN216/ ADTRG0#/ COMP4
70		P65			IRQ9	AN211/ CMPC53/DA1
71		P64			IRQ8	AN210/ CMPC33/DA0
72	AVCC2					
73	AVSS2					
74		P63			IRQ7	AN209/ CMPC23
75		P62			IRQ6	AN208/ CMPC43
76		P61			IRQ5	AN207/ CMPC13
77		P60			IRQ4	AN206/ CMPC03
78		P55			IRQ3	AN203/ CMPC32
79		P54			IRQ2	AN202/ CMPC22/ CVREFC1
80		P53			IRQ1	AN201/ CMPC12/ CVREFC0
81		P52			IRQ0	AN200/ CMPC02
82		P51				AN205/ CMPC52
83		P50				AN204/ CMPC42
84		P47				AN103
85		P46				AN102/ CMPC50/ CMPC51
86		P45				AN101/ CMPC40/ CMPC41
87		P44				AN100/ CMPC30/ CMPC31
88		P43				AN003

Table 1.5 List of Pin and Pin Functions (100-Pin LFQFP) (6/6)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
89		P42				AN002/ CMPC20/ CMPC21
90		P41				AN001/ CMPC10/ CMPC11
91		P40				AN000/ CMPC00/ CMPC01
92	AVCC1					
93	AVCC0					
94	AVSS0					
95	AVSS1					
96		P82	MTIC5U/MTIC5U#/TMO4	SCK6/SCK12	IRQ3	COMP5
97		P81	MTIC5V/MTIC5V#/TMCI4	TXD6/SMOSI6/SSDA6/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12		COMP4
98		P80	MTIC5W/MTIC5W#/TMRI4	RXD6/SMISO6/SSCL6/ RXD12/SMISO12/SSCL12/ RXDX12	IRQ5	COMP3
99		P11	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/ GTCPPO0/TOC3	SCK009/SCK008/TXDB009	IRQ1	
100		P10	MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/ GTETRGD/GTIV/TIC3	CTS6#/RTS6#/SS6#/ TXD009/TXDA009/ SMOSI009/SSDA009	IRQ0	

1.6.2 80-Pin LFQFP

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (1/5)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
1	EMLE	PN7	MTIOC9D/MTIOC9D#		IRQ5	ADST0
2	VSS					
3		P00	MTIOC9A/MTIOC9A#/ CACREF/GTIU/TIC3	RXD12/SMISO12/SSCL12/ RXDX12/RXD009/ SMISO009/SSCL009	IRQ2	ADST1/ COMP0
4	VCL					
5	MD/FINED	PN6				
6		P01	MTIOC9C/MTIOC9C#/ POE12#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTIW	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/ TXDA009/SMOSI009/ SSDA009	IRQ4	ADST2/ COMP1
7		PE4	MTCLKC/MTCLKC#/ POE10#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD	SCK009/TXDB009	IRQ1	
8		PE3	MTCLKD/MTCLKD#/ POE11#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD	CTS009#/RTS009#/SS009#/ DE009	IRQ2	
9	RES#					
10	XTAL	P37		RXD5/SMISO5/SSCL5		
11	VSS					
12	EXTAL	P36		TXD5/SMOSI5/SSDA5		
13	VCC					
14		PE2	POE10#		NMI/IRQ0	
15	TRST#	PD7	MTIOC9A/MTIOC9A#/ TMRI1/TMRI5/GTIOC0A/ GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU	TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/ SMOSI008/SSDA008/ TXDB009/SSLA1/SSL01/ CTX0	IRQ8	
16	TMS	PD6	MTIOC9C/MTIOC9C#/ TMO1/GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ GTIW	CTS1#/RTS1#/SS1#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/DE011/ SSLA0/SSL00	IRQ5	ADST0
17	TDI	PD5	TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/ GTIOC7A	RXD1/SMISO1/SSCL1/ RXD011/SMISO011/ SSCL011/SSL00	IRQ6	
18	TCK	PD4	TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#	SCK1/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02	IRQ2	
19	TDO	PD3	TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B	TXD1/SMOSI1/SSDA1/ TXD011/TXDA011/ SMOSI011/SSDA011/MOSI0		
20		PD2	TMCI1/TMO4/GTIOC2B/ GTIOC0A/GTIOC2B#/ GTIOC0A#	SCK5/SCK008/TXDB008/ MOSIA/MOSI0		

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (2/5)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
21		PB6	GTIOC2A/GTIOC3A/ GTIOC2A#/GTIOC3A#/ TOC0	RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/ RXDX12/RXD011/ SMISO011/SSCL011/MISO0/ CRX0	IRQ2	
22		PB5	GTIOC2B/GTIOC3B/ GTIOC2B#/GTIOC3B#/TIC0	TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD011/ TXDA011/SMOSI011/ SSDA011/RSPCK0/CTX0		
23	VCC					
24		PB4	POE8#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	CTS5#/RTS5#/SS5#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/SCK011/ TXDB011/MISOA/SSL01/ CRX0	IRQ3	
25	VSS					
26		PB3	MTIOC0A/MTIOC0A#/ CACREF/GTIU/TOC1	SCK6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ CTS009#/RTS009#/SS009#/ DE009/RSPCKA/CTX0	IRQ9	
27		PB2	MTIOC0B/MTIOC0B#/ TMRI0/GTADSM0/ GTIOC7A/GTIOC7A#/GTIV/ TIC1	TXD6/SMOSI6/SSDA6/ SDA0/SDA00		ADSM0
28		PB1	MTIOC0C/MTIOC0C#/ TMCI0/GTADSM1/ GTIOC7B/GTIOC7B#/GTIW/ TOC2	RXD6/SMISO6/SSCL6/ SCL0/SCL00	IRQ4	ADSM1
29		PB0	MTIOC0D/MTIOC0D#/ TMO0/TIC2	TXD6/SMOSI6/SSDA6/ TXD008/TXDA008/ SMOSI008/SSDA008/ CTS011#/RTS011#/SS011#/ DE011/MOSIA/MOSI0	IRQ8	ADTRG2#
30		PA5	MTIOC1A/MTIOC1A#/ TMCI3	RXD6/SMISO6/SSCL6/ RXD008/SMISO008/ SSCL008/MISOA/MISO0	IRQ1	ADTRG1#
31		PA3	MTIOC2A/MTIOC2A#/ TMRI7/GTADSM0	TXD009/TXDA009/ SMOSI009/SSDA009/ SCK008/TXDB008/SSLA0/ SSL00		
32	VCC					
33		P96	POE4#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO4	CTS008#/RTS008#/SS008#/ DE008/SSL03/RSPCK0	IRQ4	
34	VSS					
35		P95	MTIOC6B/MTIOC1A/ MTIOC6B#/MTIOC1A#/ TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/ GTOUUP	RXD6/SMISO6/SSCL6/ RXD008/SMISO008/ SSCL008/MISOA/SSL02/ MISO0	IRQ1	ADTRG1#

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (3/5)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
36		P94	MTIOC7A/MTIOC2A/ MTIOC7A#/MTIOC2A#/ TMRI7/GTIOC5A/ GTADSM0/GTIOC5A#/ GTOVUP	TXD009/TXDA009/ SMOSI009/SSDA009/ SCK008/TXDB008/SSLA0/ SSL00		
37		P93	MTIOC7B/MTIOC6A/ MTIOC7B#/MTIOC6A#/ TMO4/GTIOC6A/GTIOC6A#/ GTOWUP	TXD009/TXDA009/ SMOSI009/SSDA009/ RXD011/SMISO011/ SSCL011/SSLA2/SSL02/ MOSI0/CRX0	IRQ14	ADTRG0#
38		P92	MTIOC6D/MTIOC6C/ MTIOC6D#/MTIOC6C#/ TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/ GTOULO	SCK009/TXD011/TXDA011/ SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/ MISO0/CTX0		
39		P91	MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC5B#/ GTOVLO	RXD5/SMISO5/SSCL5/ RSPCK0		
40		P90	MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC6B#/ GTOWLO	TXD5/SMOSI5/SSDA5/ SSL01		
41		P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#/ GTOWLO	SSL03		
42		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#/ GTOVLO	SSL02		
43		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTOULO	SSL01		
44		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#/ GTOWUP	SSL00		
45		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#/ GTOVUP	MOSI0		
46		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#/ GTOUUP	MISO0		
47		P70	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/ RSPCK0	IRQ5	
48	VCC					
49		P31	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6/GTIU	SSLA1/SSL01	IRQ6	
50	VSS					

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (4/5)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
51		P30	MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMCI6/GTIV	SCK008/CTS008#/ RTS008#/SS008#/DE008/ SSLA0/SSL00	IRQ7	COMP3
52		P27	MTIOC1A/MTIOC0C/ MTIOC1A#/MTIOC0C#/ TMO2/TMO6/POE9#	RSPCKA/RSPCK0	IRQ15	
53		P22	MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ TMRI2/TMO4/MTIOC9B/ GTIV	RXD12/SMISO12/SSCL12/ RXDX12/RXD008/ SMISO008/SSCL008/ SCK008/TXDB008/MISOA/ MISO0/CRX0	IRQ10	ADTRG2#/ COMP2
54		P21	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4/TMO6/GTIU	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD008/ TXDA008/SMOSI008/ SSDA008/MOSIA/MOSI0	IRQ6	AN217/ ADTRG1#/ COMP5
55		P20	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4/TMO2/GTIW	CTS008#/RTS008#/SS008#/ RXD008/SMISO008/ SSCL008/DE008/RSPCKA/ RSPCK0	IRQ7	AN216/ ADTRG0#/ COMP4
56		P65			IRQ9	AN211/ CMPC53/DA1
57		P64			IRQ8	AN210/ CMPC33/DA0
58	AVCC2					
59	AVSS2					
60		P60			IRQ4	AN206/ CMPC03
61		P55			IRQ3	AN203/ CMPC32
62		P54			IRQ2	AN202/ CMPC22/ CVREFC1
63		P53			IRQ1	AN201/ CMPC12/ CVREFC0
64		P52			IRQ0	AN200/ CMPC02
65		P51				AN205/ CMPC52
66		P50				AN204/ CMPC42
67		P47				AN103
68		P46				AN102/ CMPC50/ CMPC51
69		P45				AN101/ CMPC40/ CMPC41
70		P44				AN100/ CMPC30/ CMPC31
71		P43				AN003

Table 1.6 List of Pin and Pin Functions (80-Pin LFQFP) (5/5)

Pin Number 80-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
72		P42				AN002/ CMPC20/ CMPC21
73		P41				AN001/ CMPC10/ CMPC11
74		P40				AN000/ CMPC00/ CMPC01
75	AVCC1					
76	AVCC0					
77	AVSS0					
78	AVSS1					
79		P11	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/ GTCPPO0/TOC3	SCK009/SCK008/TXDB009	IRQ1	
80		P10	MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/ GTETRGD/GTIV/TIC3	CTS6#/RTS6#/SS6#/ TXD009/TXDA009/ SMOSI009/SSDA009	IRQ0	

1.6.3 64-Pin LFQFP, 64-Pin HWQFN (Products with 64 Kbytes of RAM)

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP, 64-Pin HWQFN) (Products with 64 Kbytes of RAM) (1/4)

Pin Number 64-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
1	EMLE	PN7	MTIOC9D/MTIOC9D#		IRQ5	ADST0
2		P00	MTIOC9A/MTIOC9A#/ CACREF/GTIU/TIC3	RXD12/SMISO12/SSCL12/ RXDX12/RXD009/ SMISO009/SSCL009	IRQ2	ADST1/ COMP0
3	VCL					
4	MD/FINED	PN6				
5		P01	MTIOC9C/MTIOC9C#/ POE12#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTIW	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/ TXDA009/SMOSI009/ SSDA009	IRQ4	ADST2/ COMP1
6	RES#					
7	XTAL	P37		RXD5/SMISO5/SSCL5		
8	VSS					
9	EXTAL	P36		TXD5/SMOSI5/SSDA5		
10	VCC					
11		PE2	POE10#		NMI/IRQ0	
12	TRST#	PD7	MTIOC9A/MTIOC9A#/ TMRI1/TMRI5/GTIOC0A/ GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU	TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/ SMOSI008/SSDA008/ TXDB009/SSLA1/SSL01/ CTX0	IRQ8	
13	TMS	PD6	MTIOC9C/MTIOC9C#/ TMO1/GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ GTIW	CTS1#/RTS1#/SS1#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/DE011/ SSLA0/SSL00	IRQ5	ADST0
14	TDI	PD5	TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/ GTIOC7A	RXD1/SMISO1/SSCL1/ RXD011/SMISO011/ SSCL011/SSL00	IRQ6	
15	TCK	PD4	TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#	SCK1/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02	IRQ2	
16	TDO	PD3	TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B	TXD1/SMOSI1/SSDA1/ TXD011/TXDA011/ SMOSI011/SSDA011/MOSI0		
17		PB6	GTIOC2A/GTIOC3A/ GTIOC2A#/GTIOC3A#/ TOC0	RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/ RXDX12/RXD011/ SMISO011/SSCL011/MISO0/ CRX0	IRQ2	
18		PB5	GTIOC2B/GTIOC3B/ GTIOC2B#/GTIOC3B#/TIC0	TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD011/ TXDA011/SMOSI011/ SSDA011/RSPCK0/CTX0		

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP, 64-Pin HWQFN) (Products with 64 Kbytes of RAM) (2/4)

Pin Number 64-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
19		PB4	POE8#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	CTS5#/RTS5#/SS5#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/SCK011/ TXDB011/MISOA/SSL01/ CRX0	IRQ3	
20		PB3	MTIOC0A/MTIOC0A#/ CACREF/GTIU/TOC1	SCK6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ CTS009#/RTS009#/SS009#/ DE009/RSPCKA/CTX0	IRQ9	
21		PB2	MTIOC0B/MTIOC0B#/ TMRI0/GTADSM0/ GTIOC7A/GTIOC7A#/GTIV/ TIC1	TXD6/SMOSI6/SSDA6/ SDA0/SDA00		ADSM0
22		PB1	MTIOC0C/MTIOC0C#/ TMCI0/GTADSM1/ GTIOC7B/GTIOC7B#/GTIW/ TOC2	RXD6/SMISO6/SSCL6/ SCL0/SCL00	IRQ4	ADSM1
23		PB0	MTIOC0D/MTIOC0D#/ TMO0/TIC2	TXD6/SMOSI6/SSDA6/ TXD008/TXDA008/ SMOSI008/SSDA008/ CTS011#/RTS011#/SS011#/ DE011/MOSIA/MOSI0	IRQ8	ADTRG2#
24	VCC					
25		P96	POE4#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO4	CTS008#/RTS008#/SS008#/ DE008/SSL03/RSPCK0	IRQ4	
26	VSS					
27		P95	MTIOC6B/MTIOC1A/ MTIOC6B#/MTIOC1A#/ TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/ GTOUUP	RXD6/SMISO6/SSCL6/ RXD008/SMISO008/ SSCL008/MISOA/SSL02/ MISO0	IRQ1	ADTRG1#
28		P94	MTIOC7A/MTIOC2A/ MTIOC7A#/MTIOC2A#/ TMRI7/GTIOC5A/ GTADSM0/GTIOC5A#/ GTOVUP	TXD009/TXDA009/ SMOSI009/SSDA009/ SCK008/TXDB008/SSLA0/ SSL00		
29		P93	MTIOC7B/MTIOC6A/ MTIOC7B#/MTIOC6A#/ TMO4/GTIOC6A/GTIOC6A#/ GTOWUP	TXD009/TXDA009/ SMOSI009/SSDA009/ RXD011/SMISO011/ SSCL011/SSLA2/SSL02/ MOSI0/CRX0	IRQ14	ADTRG0#
30		P92	MTIOC6D/MTIOC6C/ MTIOC6D#/MTIOC6C#/ TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/ GTOULO	SCK009/TXD011/TXDA011/ SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/ MISO0/CTX0		
31		P91	MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC5B#/ GTOVLO	RXD5/SMISO5/SSCL5/ RSPCK0		
32		P90	MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC6B#/ GTOWLO	TXD5/SMOSI5/SSDA5/ SSL01		

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP, 64-Pin HWQFN) (Products with 64 Kbytes of RAM) (3/4)

Pin Number 64-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
33		P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#/ GTOWLO	SSL03		
34		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#/ GTOVLO	SSL02		
35		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTOULO	SSL01		
36		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#/ GTOWUP	SSL00		
37		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#/ GTOVUP	MOSI0		
38		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#/ GTOUUP	MISO0		
39		P70	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/ RSPCK0	IRQ5	
40	VCC					
41	VSS					
42		P22	MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ TMRI2/TMO4/MTIOC9B/ GTIV	RXD12/SMISO12/SSCL12/ RXDX12/RXD008/ SMISO008/SSCL008/ SCK008/TXDB008/MISOA/ MISO0/CRX0	IRQ10	ADTRG2#/ COMP2
43		P21	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4/TMO6/GTIU	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD008/ TXDA008/SMOSI008/ SSDA008/MOSIA/MOSI0	IRQ6	AN217/ ADTRG1#/ COMP5
44		P20	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4/TMO2/GTIW	CTS008#/RTS008#/SS008#/ RXD008/SMISO008/ SSCL008/DE008/RSPCKA/ RSPCK0	IRQ7	AN216/ ADTRG0#/ COMP4
45		P65			IRQ9	AN211/ CMPC53/DA1
46		P64			IRQ8	AN210/ CMPC33/DA0
47	AVCC2					
48	AVSS2					
49		P54			IRQ2	AN202/ CMPC22/ CVREFC1

Table 1.7 List of Pin and Pin Functions (64-Pin LFQFP, 64-Pin HWQFN) (Products with 64 Kbytes of RAM) (4/4)

Pin Number 64-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
50		P53			IRQ1	AN201/ CMPC12/ CVREFC0
51		P52			IRQ0	AN200/ CMPC02
52		P47				AN103
53		P46				AN102/ CMPC50/ CMPC51
54		P45				AN101/ CMPC40/ CMPC41
55		P44				AN100/ CMPC30/ CMPC31
56		P43				AN003
57		P42				AN002/ CMPC20/ CMPC21
58		P41				AN001/ CMPC10/ CMPC11
59		P40				AN000/ CMPC00/ CMPC01
60	AVCC1					
61	AVCC0					
62	AVSS0					
63	AVSS1					
64		P11	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/ GTCPPO0/TOC3	SCK009/SCK008/TXDB009	IRQ1	

1.6.4 64-Pin LFQFP (Products with 48 Kbytes of RAM)

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (Products with 48 Kbytes of RAM) (1/4)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
1	EMLE	PN7	MTIOC9D/MTIOC9D#		IRQ5	ADST0
2		P00	MTIOC9A/MTIOC9A#/ CACREF/GTIU/TIC3	RXD12/SMISO12/SSCL12/ RXDX12	IRQ2	COMP0
3	VCL					
4	MD/FINED	PN6				
5		P01	MTIOC9C/MTIOC9C#/ POE12#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTIW	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12	IRQ4	ADST2/ COMP1
6	RES#					
7	XTAL	P37		RXD5/SMISO5/SSCL5		
8	VSS					
9	EXTAL	P36		TXD5/SMOSI5/SSDA5		
10	VCC					
11		PE2	POE10#		NMI/IRQ0	
12	TRST#	PD7	MTIOC9A/MTIOC9A#/ TMRI1/TMRI5/GTIOC0A/ GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU	TXD5/SMOSI5/SSDA5/ SSLA1/CTX0	IRQ8	
13	TMS	PD6	MTIOC9C/MTIOC9C#/ TMO1/GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ GTIW	CTS1#/RTS1#/SS1#/ RXD12/SMISO12/SSCL12/ RXDX12/SSLA0	IRQ5	ADST0
14	TDI	PD5	TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/ GTIOC7A	RXD1/SMISO1/SSCL1	IRQ6	
15	TCK	PD4	TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#	SCK1/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12	IRQ2	
16	TDO	PD3	TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B	TXD1/SMOSI1/SSDA1		
17		PB6	GTIOC2A/GTIOC3A/ GTIOC2A#/GTIOC3A#/ TOC0	RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/ RXDX12/CRX0	IRQ2	
18		PB5	GTIOC2B/GTIOC3B/ GTIOC2B#/GTIOC3B#/TIC0	TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0		
19		PB4	POE8#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	CTS5#/RTS5#/SS5#/ RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0	IRQ3	
20		PB3	MTIOC0A/MTIOC0A#/ CACREF/GTIU/TOC1	SCK6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ RSPCKA/CTX0	IRQ9	
21		PB2	MTIOC0B/MTIOC0B#/ TMRI0/GTADSM0/ GTIOC7A/GTIOC7A#/GTIV/ TIC1	TXD6/SMOSI6/SSDA6/ SDA0		ADSM0
22		PB1	MTIOC0C/MTIOC0C#/ TMCI0/GTADSM1/ GTIOC7B/GTIOC7B#/GTIW/ TOC2	RXD6/SMISO6/SSCL6/SCL0	IRQ4	ADSM1

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (Products with 48 Kbytes of RAM) (2/4)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
23		PB0	MTIOC0D/MTIOC0D#/ TMO0/TIC2	TXD6/SMOSI6/SSDA6/ MOSIA	IRQ8	ADTRG2#
24	VCC					
25		P96	POE4#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO4		IRQ4	
26	VSS					
27		P95	MTIOC6B/MTIOC1A/ MTIOC6B#/MTIOC1A#/ TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/ GTOUUP	RXD6/SMISO6/SSCL6/ MISOA	IRQ1	
28		P94	MTIOC7A/MTIOC2A/ MTIOC7A#/MTIOC2A#/ TMRI7/GTIOC5A/ GTADSM0/GTIOC5A#/ GTOVUP	SSLA0		
29		P93	MTIOC7B/MTIOC6A/ MTIOC7B#/MTIOC6A#/ TMO4/GTIOC6A/GTIOC6A#/ GTOWUP	SSLA2/CRX0	IRQ14	ADTRG0#
30		P92	MTIOC6D/MTIOC6C/ MTIOC6D#/MTIOC6C#/ TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/ GTOULO	SSLA3/CTX0		
31		P91	MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC5B#/ GTOVLO	RXD5/SMISO5/SSCL5		
32		P90	MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC6B#/ GTOWLO	TXD5/SMOSI5/SSDA5		
33		P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#/ GTOWLO			
34		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#/ GTOVLO			
35		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTOULO			
36		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#/ GTOWUP			
37		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#/ GTOVUP			
38		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#/ GTOUUP			

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (Products with 48 Kbytes of RAM) (3/4)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
39		P70	MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	SCK5/SSLA0	IRQ5	
40	VCC					
41	VSS					
42		P22	MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ TMRI2/TMO4/MTIOC9B/ GTIV	RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0	IRQ10	ADTRG2#/ COMP2
43		P21	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4/TMO6/GTIU	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA	IRQ6	AN217/ COMP5
44		P20	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4/TMO2/GTIW	RSPCKA	IRQ7	AN216/ ADTRG0#/ COMP4
45		P65			IRQ9	AN211/ CMPC53/DA1
46		P64			IRQ8	AN210/ CMPC52/DA0
47	AVCC2					
48	AVSS2					
49		P54			IRQ2	AN202/ CMPC22/ CVREFC1
50		P53			IRQ1	AN201/ CMPC12/ CVREFC0
51		P52			IRQ0	AN200/ CMPC02
52		P47				AN206/ CMPC03
53		P46				AN006/ CMPC21
54		P45				AN005/ CMPC11
55		P44				AN004/ CMPC01
56		P43				AN003/ CMPC23/ CMPC50
57		P42				AN002/ CMPC20
58		P41				AN001/ CMPC10
59		P40				AN000/ CMPC13/ CMPC00
60	NC					
61	AVCC0					
62	AVSS0					

Table 1.8 List of Pin and Pin Functions (64-Pin LFQFP) (Products with 48 Kbytes of RAM) (4/4)

Pin Number 64-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
63	NC					
64		P11	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/ GTCPPO0/TOC3		IRQ1	

1.6.5 48-Pin LFQFP, 48-Pin HWQFN (Products with 64 Kbytes of RAM)

Table 1.9 List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (Products with 64 Kbytes of RAM) (1/3)

Pin Number 48-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
1		P00	MTIOC9A/MTIOC9A#/ CACREF/GTIU/TIC3	RXD12/SMISO12/SSCL12/ RXDX12/RXD009/ SMISO009/SSCL009	IRQ2	ADST1/ COMP0
2	VCL					
3	MD/FINED	PN6				
4	RES#					
5	XTAL	P37		RXD5/SMISO5/SSCL5		
6	VSS					
7	EXTAL	P36		TXD5/SMOSI5/SSDA5		
8	VCC					
9		PE2	POE10#		NMI/IRQ0	
10	TRST#	PD7	MTIOC9A/MTIOC9A#/ TMRI1/TMRI5/GTIOC0A/ GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU	TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/ SMOSI008/SSDA008/ TXDB009/SSLA1/SSL01/ CTX0	IRQ8	
11	TDI	PD5	TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/ GTIOC7A	RXD1/SMISO1/SSCL1/ RXD011/SMISO011/ SSCL011/SSL00	IRQ6	
12	TDO	PD3	TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B	TXD1/SMOSI1/SSDA1/ TXD011/TXDA011/ SMOSI011/SSDA011/MOSI0		
13		PB6	GTIOC2A/GTIOC3A/ GTIOC2A#/GTIOC3A#/ TOC0	RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/ RXDX12/RXD011/ SMISO011/SSCL011/MISO0/ CRX0	IRQ2	
14		PB5	GTIOC2B/GTIOC3B/ GTIOC2B#/GTIOC3B#/TIC0	TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD011/ TXDA011/SMOSI011/ SSDA011/RSPCK0/CTX0		
15		PB4	POE8#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	CTS5#/RTS5#/SS5#/ RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/ RTS011#/SS011#/SCK011/ TXDB011/MISOA/SSL01/ CRX0	IRQ3	
16		PB3	MTIOC0A/MTIOC0A#/ CACREF/GTIU/TOC1	SCK6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ CTS009#/RTS009#/SS009#/ DE009/RSPCKA/CTX0	IRQ9	
17		PB2	MTIOC0B/MTIOC0B#/ TMRI0/GTADSM0/ GTIOC7A/GTIOC7A#/GTIV/ TIC1	TXD6/SMOSI6/SSDA6/ SDA0/SDA00		ADSM0
18		PB1	MTIOC0C/MTIOC0C#/ TMCI0/GTADSM1/ GTIOC7B/GTIOC7B#/GTIW/ TOC2	RXD6/SMISO6/SSCL6/ SCL0/SCL00	IRQ4	ADSM1

Table 1.9 List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (Products with 64 Kbytes of RAM) (2/3)

Pin Number 48-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
19		PB0	MTIOC0D/MTIOC0D#/ TMO0/TIC2	TXD6/SMOSI6/SSDA6/ TXD008/TXDA008/ SMOSI008/SSDA008/ CTS011#/RTS011#/SS011#/ DE011/MOSIA/MOSI0	IRQ8	ADTRG2#
20		P95	MTIOC6B/MTIOC1A/ MTIOC6B#/MTIOC1A#/ TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/ GTOUUP	RXD6/SMISO6/SSCL6/ RXD008/SMISO008/ SSCL008/MISOA/SSL02/ MISO0	IRQ1	ADTRG1#
21		P94	MTIOC7A/MTIOC2A/ MTIOC7A#/MTIOC2A#/ TMRI7/GTIOC5A/ GTADSM0/GTIOC5A#/ GTOVUP	TXD009/TXDA009/ SMOSI009/SSDA009/ SCK008/TXDB008/SSLA0/ SSL00		
22		P93	MTIOC7B/MTIOC6A/ MTIOC7B#/MTIOC6A#/ TMO4/GTIOC6A/GTIOC6A#/ GTOWUP	TXD009/TXDA009/ SMOSI009/SSDA009/ RXD011/SMISO011/ SSCL011/SSLA2/SSL02/ MOSI0/CRX0	IRQ14	ADTRG0#
23		P92	MTIOC6D/MTIOC6C/ MTIOC6D#/MTIOC6C#/ TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/ GTOULO	SCK009/TXD011/TXDA011/ SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/ MISO0/CTX0		
24		P91	MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC5B#/ GTOVLO	RXD5/SMISO5/SSCL5/ RSPCK0		
25		P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#/ GTOWLO	SSL03		
26		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#/ GTOVLO	SSL02		
27		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTOULO	SSL01		
28		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#/ GTOWUP	SSL00		
29		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#/ GTOVUP	MOSI0		
30		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#/ GTOUUP	MISO0		
31	VCC					
32	VSS					

Table 1.9 List of Pin and Pin Functions (48-Pin LFQFP, 48-Pin HWQFN) (Products with 64 Kbytes of RAM) (3/3)

Pin Number 48-Pin LFQFP, HWQFN	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSCI, RSPI, RSPIA, RIIC, RI3C, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
33		P21	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4/TMO6/GTIU	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD008/ TXDA008/SMOSI008/ SSDA008/MOSIA/MOSI0	IRQ6	AN217/ ADTRG1#/ COMP5
34		P20	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4/TMO2/GTIW	CTS008#/RTS008#/SS008#/ RXD008/SMISO008/ SSCL008/DE008/RSPCKA/ RSPCK0	IRQ7	AN216/ ADTRG0#/ COMP4
35	AVCC2					
36	AVSS2					
37		P62			IRQ6	AN208/ CMPC43
38		P53			IRQ1	AN201/ CMPC12/ CVREFC0
39		P52			IRQ0	AN200/ CMPC02
40		P44				AN100/ CMPC30/ CMPC31
41		P43				AN003
42		P42				AN002/ CMPC20/ CMPC21
43		P41				AN001/ CMPC10/ CMPC11
44		P40				AN000/ CMPC00/ CMPC01
45	AVCC0/ AVCC1					
46	AVSS0/AVSS1					
47		P11	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/ GTCPPO0/TOC3	SCK009/SCK008/TXDB009	IRQ1	
48		P10	MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/ GTETRGD/GTIV/TIC3	CTS6#/RTS6#/SS6#/ TXD009/TXDA009/ SMOSI009/SSDA009	IRQ0	

1.6.6 48-Pin LFQFP (Products with 48 Kbytes of RAM)

Table 1.10 List of Pin and Pin Functions (48-Pin LFQFP) (Products with 48 Kbytes of RAM) (1/3)

Pin Number 48-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
1		P00	MTIOC9A/MTIOC9A#/ CACREF/GTIU/TIC3	RXD12/SMISO12/SSCL12/ RXDX12	IRQ2	COMP0
2	VCL					
3	MD/FINED	PN6				
4	RES#					
5	XTAL	P37		RXD5/SMISO5/SSCL5		
6	VSS					
7	EXTAL	P36		TXD5/SMOSI5/SSDA5		
8	VCC					
9		PE2	POE10#		NMI/IRQ0	
10	TRST#	PD7	MTIOC9A/MTIOC9A#/ TMRI1/TMRI5/GTIOC0A/ GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU	TXD5/SMOSI5/SSDA5/ SSLA1/CTX0	IRQ8	
11	TDI	PD5	TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/ GTIOC7A	RXD1/SMISO1/SSCL1	IRQ6	
12	TDO	PD3	TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B	TXD1/SMOSI1/SSDA1		
13		PB6	GTIOC2A/GTIOC3A/ GTIOC2A#/GTIOC3A#/ TOC0	RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/ RXDX12/CRX0	IRQ2	
14		PB5	GTIOC2B/GTIOC3B/ GTIOC2B#/GTIOC3B#/TIC0	TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0		
15		PB4	POE8#/GTETRGA/ GTETRGB/GTETRGC/ GTETRGD/GTCPPO0	CTS5#/RTS5#/SS5#/ RXD12/SMISO12/SSCL12/ RXDX12/MISOA/CRX0	IRQ3	
16		PB3	MTIOC0A/MTIOC0A#/ CACREF/GTIU/TOC1	SCK6/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/ RSPCKA/CTX0	IRQ9	
17		PB2	MTIOC0B/MTIOC0B#/ TMRI0/GTADSM0/ GTIOC7A/GTIOC7A#/GTIV/ TIC1	TXD6/SMOSI6/SSDA6/ SDA0		ADSM0
18		PB1	MTIOC0C/MTIOC0C#/ TMCI0/GTADSM1/ GTIOC7B/GTIOC7B#/GTIW/ TOC2	RXD6/SMISO6/SSCL6/SCL0	IRQ4	ADSM1
19		PB0	MTIOC0D/MTIOC0D#/ TMO0/TIC2	TXD6/SMOSI6/SSDA6/ MOSIA	IRQ8	ADTRG2#
20		P95	MTIOC6B/MTIOC1A/ MTIOC6B#/MTIOC1A#/ TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/ GTOUUP	RXD6/SMISO6/SSCL6/ MISOA	IRQ1	

Table 1.10 List of Pin and Pin Functions (48-Pin LFQFP) (Products with 48 Kbytes of RAM) (2/3)

Pin Number 48-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
21		P94	MTIOC7A/MTIOC2A/ MTIOC7A#/MTIOC2A#/ TMRI7/GTIOC5A/ GTADSM0/GTIOC5A#/ GTOVUP	SSLA0		
22		P93	MTIOC7B/MTIOC6A/ MTIOC7B#/MTIOC6A#/ TMO4/GTIOC6A/GTIOC6A#/ GTOWUP	SSLA2/CRX0	IRQ14	ADTRG0#
23		P92	MTIOC6D/MTIOC6C/ MTIOC6D#/MTIOC6C#/ TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/ GTOULO	SSLA3/CTX0		
24		P91	MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC5B#/ GTOVLO	RXD5/SMISO5/SSCL5		
25		P76	MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B#/ GTOWLO			
26		P75	MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B#/ GTOVLO			
27		P74	MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B#/ GTOULO			
28		P73	MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A#/ GTOWUP			
29		P72	MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A#/ GTOVUP			
30		P71	MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A#/ GTOUUP			
31	VCC					
32	VSS					
33		P21	MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMCI4/TMO6/GTIU	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/MOSIA	IRQ6	AN217/ COMP5
34		P20	MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4/TMO2/GTIW	RSPCKA	IRQ7	AN216/ ADTRG0#/ COMP4
35	AVCC2					
36	AVSS2					
37		P62			IRQ6	AN208/ CMPC51

Table 1.10 List of Pin and Pin Functions (48-Pin LFQFP) (Products with 48 Kbytes of RAM) (3/3)

Pin Number 48-Pin LFQFP	Power Supply Clock System Control	I/O Port	Timer (MTU, GPTW, TMR, POE, POEG, CAC, CMTW)	Communications (SCI, RSPI, RIIC, CANFD)	Interrupt (IRQ, NMI)	Analog (A/D, D/A, CMPC)
38		P53			IRQ1	AN201/ CMPC12/ CVREFC0
39		P52			IRQ0	AN200/ CMPC02
40		P44				AN004/ CMPC01
41		P43				AN003/ CMPC23/ CMPC50
42		P42				AN002/ CMPC20
43		P41				AN001/ CMPC10
44		P40				AN000/ CMPC13/ CMPC00
45	AVCC0					
46	AVSS0					
47		P11	MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/ GTIOC3B#/GTETRGC/ GTCPPO0/TOC3		IRQ1	
48		P10	MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/ GTETRGD/GTIV/TIC3	CTS6#/RTS6#/SS6#	IRQ0	

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = 0V

Item		Symbol	Value	Unit
Power supply voltage*1		VCC	–0.3 to +6.5	V
Analog power supply voltage*1		AVCC0, AVCC1, AVCC2	–0.3 to +6.5	V
Input voltage	PB1 and PB2	V_{in}	–0.3 to +6.5	V
	P40 to P47, P50 to P55, and P60 to P65		–0.3 to AVCC2 + 0.3 (up to 6.5)	
	Other than above		–0.3 to VCC + 0.3 (up to 6.5)	
Junction temperature		T_j	–40 to +125	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Insert capacitors with good frequency characteristics between each power supply pin and the ground. Specifically, place capacitors with a value around 0.1 µF as close as possible to every power supply pin, and use the shortest and thickest possible traces.

2.2 Recommended operating conditions

Table 2.2 Recommended operating conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage		VCC*1	2.7	—	5.5	V
		VSS	—	0	—	
Analog power supply voltage*2		AVCC0, AVCC1, AVCC2*1	3.0	—	5.5	V
		AVSS0, AVSS1, AVSS2	—	0	—	
Input voltage	PB1, PB2	V_{in}	–0.3	—	5.8	V
	P40 to P47, P50 to P55, and P60 to P65		–0.3	—	AVCC2 + 0.3	
	Other than above		–0.3	—	VCC + 0.3	
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	
Junction temperature	D version	T_j	–40	—	105	°C
	G version		–40	—	125	

Note 1. Comply with the following voltage condition: VCC ≤ AVCC0 = AVCC1 = AVCC2

Note 2. When not using any of the12-bit A/D converter (unit 0 to 2), 12-bit D/A converter, comparator C, or temperature sensor, connect AVCC0, AVCC1, and AVCC2 to VCC, and AVSS0, AVSS1, and AVSS2 to VSS, respectively. For details, refer to section 42.6.9, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Table 2.3 Recommended operating conditions (2)

Item	Symbol	Value
Decoupling capacitance to stabilize the internal voltage	C_{VCL}	0.47 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.47 µF and a capacitance tolerance is ±30% or better.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CANFD input pin MTU input pin GPTW input pin POE input pin POEG input pin TMR input pin SCI input pin RSCI input pin ADTRG# input pin RES#, NMI	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	IRQ input pin (except for P52 to P55, and P60 to P65)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	IRQ input pin (P52 to P55, and P60 to P65)	V_{IH}	0.8 × AVCC2	—	—		
		V_{IL}	—	—	0.2 × AVCC2		
		ΔV_T	0.06 × AVCC2	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—		
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	RI3C input pin	V_{IH}	0.7 × VCC	—	—		VCC = 2.7 to 3.6 V
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.1 × VCC	—	—		
	Pins for 5 V tolerant (PB1 and PB2)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	Analog input pins (P40 to P47, P50 to P55, and P60 to P63)	V_{IH}	0.8 × AVCC2	—	—		
		V_{IL}	—	—	0.2 × AVCC2		
	Other input pins (pins other than those above)	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
High-level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	—	V	
	EXTAL, RSPI input pin, RSPIA input pin		0.8 × VCC	—	—		
	RIIC (SMBus)		2.1	—	—		
Low-level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	0.1 × VCC	V	
	EXTAL, RSPI input pin, RSPIA input pin		—	—	0.2 × VCC		
	RIIC (SMBus)		—	—	0.8		

Table 2.5 DC Characteristics (2)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	P40 to P47, P50 to P55, and P60 to P65		V_{OH}	AVCC2 – 0.5	—	—	V	I_{OH} = –1.0 mA
	P90 to P95, P71 to P76, P81, PB5, and PD3			VCC – 1.0	—	—		I_{OH} = –5.0 mA VCC < 4.0 V (when the large current output is set)
				VCC – 1.1	—	—		I_{OH} = –15.0 mA VCC ≥ 4.0 V (when the large current output is set)
	RI3C pins			VCC – 0.27	—	—		I_{OH} = –3.0 mA
	Other than above	Normal drive		VCC – 0.5	—	—		I_{OH} = –1.0 mA
		High drive		VCC – 0.5	—	—		I_{OH} = –2.0 mA
Low-level output voltage	P40 to P47, P50 to P55, and P60 to P65		V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	P90 to P95, P71 to P76, P81, PB5, and PD3			—	—	1.0		I_{OL} = 15.0 mA (when the large current output is set)
	RIIC pins			—	—	0.4		I_{OL} = 3.0 mA
				—	—	0.6		I_{OL} = 6.0 mA
	RI3C pins			—	—	0.27		I_{OL} = 3.0 mA
	Other than above	Normal drive		—	—	0.5		I_{OL} = 1.0 mA
		High drive		—	—	0.5		I_{OL} = 2.0 mA
Input leakage current	RES#, MD pin, PE2, and EMLE*1		$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	RIIC pins		$\lvert I_{TSI} \rvert$	—	—	5.0	μA	V_{in} = 0 V V_{in} = VCC
	Other than above			—	—	1.0		
Input pull-up resistors	P40 to P47, P50 to P55, and P60 to P65		R_{PU}	10	—	100	kΩ	AVCC2 = 3.0 to 5.5 V V_{in} = 0 V
	Pins other than those above and PE2			10	—	100		VCC = 2.7 to 5.5 V V_{in} = 0 V
Input pull-down resistors	EMLE		R_{PD}	10	—	100	kΩ	V_{in} = VCC = AVCC
Input capacitance	RIIC pins		C_{in}	—	—	16	pF	V_{bias} = 0 V V_{amp} = 20 mV f = 1 MHz T_a = 25°C
	Other than above			—	—	8		
Output voltage of the VCL pin			V_{CL}	—	1.25	—	V	

Note 1. The input leakage current value at the EMLE pin is only when V_{in} = 0 V.

Table 2.6 DC Characteristics (3) (Products with 64 Kbytes of RAM)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	Normal operating mode	Full operation*2		I_{CC}*3	—	66	—	74	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 120 MHz PCLKD = 60 MHz FCLK = 60 MHz
		Normal operation	Peripheral module clocks are supplied*4		22	—	22	—		
			Peripheral module clocks are stopped*4, *5		11	—	11	—		
		CoreMark	Peripheral module clocks are stopped*4, *5		18	—	18	—		
		Sleep mode: Peripheral module clocks are supplied*4			18	36	18	44		
		All module clock stop mode (reference value)			8.1	22	8.1	29		
		Increase current by BGO operation*6			16	—	16	—		
		Increase current by operating Trusted Secure IP			4.3	5.2	4.3	5.2		
	Software standby mode				0.9	8	0.9	13		

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows.
• D version product
I_{CC} Max. = 0.417 × f + 16 (full operation in normal operating mode)
I_{CC} Typ. = 0.144 × f + 5 (normal operation in normal operating mode)
I_{CC} Max. = 0.167 × f + 16 (sleep mode)
• G version product
I_{CC} Max. = 0.433 × f + 22 (full operation in normal operating mode)
I_{CC} Typ. = 0.144 × f + 5 (normal operation in normal operating mode)
I_{CC} Max. = 0.183 × f + 22 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are the same.
Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 2.7 DC Characteristics (3) (Products with 48 Kbytes of RAM)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	Normal operating mode	Full operation*2		I_{CC}*3	—	47	—	52	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 120 MHz PCLKD = 60 MHz FCLK = 60 MHz
		Normal operation	Peripheral module clocks are supplied*4		17	—	17	—		
			Peripheral module clocks are stopped*4, *5		10	—	10	—		
		CoreMark	Peripheral module clocks are stopped*4, *5		16	—	16	—		
		Sleep mode: Peripheral module clocks are supplied*4			13	25	13	29		
		All module clock stop mode (reference value)			7.4	16	7.4	20		
		Increase current by BGO operation*6			12	—	12	—		
	Software standby mode				0.9	5	0.9	8		

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).
Note 3. I_{CC} depends on f (ICLK) as follows.
• D version product
I_{CC} Max. = 0.283 × f + 13 (full operation in normal operating mode)
I_{CC} Typ. = 0.107 × f + 4.3 (normal operation in normal operating mode)
I_{CC} Max. = 0.100 × f + 13 (sleep mode)
• G version product
I_{CC} Max. = 0.285 × f + 17.8 (full operation in normal operating mode)
I_{CC} Typ. = 0.107 × f + 4.3 (normal operation in normal operating mode)
I_{CC} Max. = 0.093 × f + 17.8 (sleep mode)
Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are the same.
Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 2.8 DC Characteristics (4)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	Unit 0	During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: enabled for all channels)	AI_{CC}	—	2.7	6.1	mA	IAVCC0_AD + SH + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: disabled for all channels)		—	2.0	3.0		IAVCC0_AD + SH
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: enabled for all channels)		—	1.9	5.0		IAVCC0_AD + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: disabled for all channels)		—	1.0	1.5		IAVCC0_AD
	Unit 1	During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: enabled for all channels)		—	2.7	6.1		IAVCC1_AD + SH + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: disabled for all channels)		—	2.0	3.0		IAVCC1_AD + SH
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: enabled for all channels)		—	1.9	5.0		IAVCC1_AD + PGA
		During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: disabled for all channels)		—	1.0	1.5		IAVCC1_AD
	Unit 2	During 12-bit A/D conversion with the temperature sensor operating		—	1.0	1.5		IAVCC2_AD + TEMP
		During 12-bit A/D conversion with the temperature sensor stopped		—	0.9	1.4		IAVCC2_AD
	Comparator (6 channels)			—	0.6	0.8		IAVCC2_CMP
	During 12-bit D/A conversion (2 channels)			—	0.6	0.8		IAVCC2_DA
	Waiting for 12-bit A/D, 12-bit D/A, Comparator C, and temperature sensor conversion (all units)			—	0.05	0.1		IAVCC0_AD + IAVCC1_AD + IAVCC2_AD + IAVCC2_DA
	12-bit A/D, 12-bit D/A, Comparator C, and temperature sensor are in module stop status (all units)			—	0.3	11.1	μA	IAVCC0_AD + IAVCC1_AD + IAVCC2_AD + IAVCC2_DA
RAM retention voltage			V_{RAM}	2.7	—	—	V	

Table 2.9 DC Characteristics (5)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC ramp rate at power-on	At normal startup	SrVCC	0.02	—	8	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	20		
VCC ramp rate at power fluctuation		dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

Note 1. When OFS1.LVDAS = 0.
Note 2. Settings of the OFS1 register are not read in boot mode, so turn on the power supply voltage with a ramp rate at normal startup.

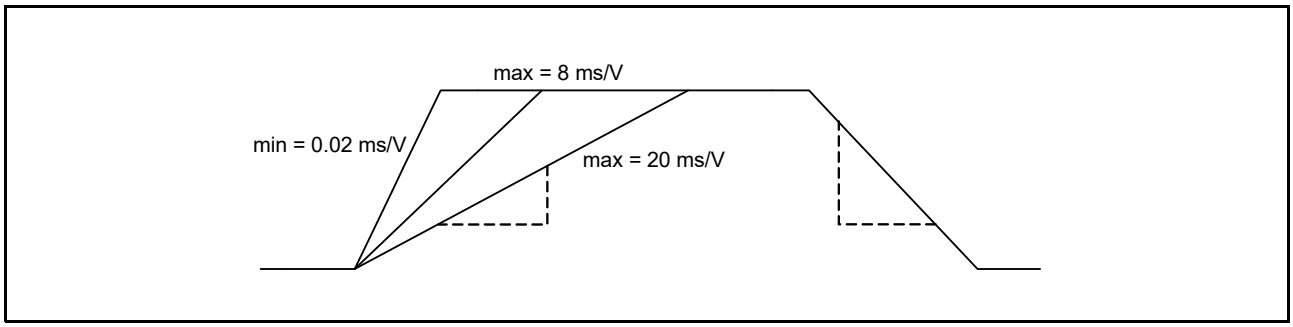


Figure 2.1 VCC Ramp Rate at Power-On

Table 2.10 Permissible Output Currents

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible low-level output current (average value per pin)	All output pins (except for RIIC pins, P40 to P47, P50 to P55, and P60 to P65)	Normal drive*1	I_{OL}	—	—	2.0	mA
		High drive*2		—	—	2.0	
		Large current output*3		—	—	15.0	
	RIIC pins	Standard mode		—	—	3	
		Fast mode		—	—	6	
	P40 to P47, P50 to P55, and P60 to P65			—	—	2.0	
Permissible low-level output current (max. value per pin)	All output pins (except for RIIC pins, P40 to P47, P50 to P55, and P60 to P65)	Normal drive*1		—	—	4.0	
		High drive*2		—	—	4.0	
		High drive*2, *4		—	—	15.0	
		Large current output*3		—	—	15.0	
	RIIC pins	Standard mode		—	—	3	
		Fast mode		—	—	6	
	P40 to P47, P50 to P55, and P60 to P65			—	—	4.0	
Permissible low-level output current (total)	Total of all output pins		ΣI_{OL}	—	—	110	mA
Permissible high-level output current (average value per pin)	All output pins (except for P40 to P47, P50 to P55, and P60 to P65)	Normal drive*1	I_{OH}	—	—	–2.0	mA
		High drive*2		—	—	–2.0	
		Large current output*3		—	—	–5.0	
		Large current output*3, *5		—	—	–15.0	
	P40 to P47, P50 to P55, and P60 to P65			—	—	–2.0	
Permissible high-level output current (max. value per pin)	All output pins (except for P40 to P47, P50 to P55, and P60 to P65)	Normal drive*1		—	—	–4.0	
		High drive*2		—	—	–4.0	
		Large current output*3		—	—	–5.0	
		Large current output*3, *5		—	—	–15.0	
	P40 to P47, P50 to P55, and P60 to P65			—	—	–4.0	
Permissible high-level output current (total)	Total of all output pins		ΣI_{OH}	—	—	–35	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. The listed value applies when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. The listed value applies when high driving ability is set with a pin for which normal driving ability is selectable, or when the pin to which high driving ability is fixed is in use.

Note 3. The listed value applies when large current output is set with a pin for which large current output ability is selectable.

Note 4. The listed value applies when VCC is at least 4.5 V.

Note 5. The listed value applies when VCC is at least 4.0 V.

Table 2.11 Standard Output Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = AVCC2 = 5.0 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Normal drive output (all output pins)	V_{OH}	—	4.97	—	V	I_{OH} = –0.5 mA
			—	4.94	—		I_{OH} = –1.0 mA
			—	4.87	—		I_{OH} = –2.0 mA
			—	4.74	—		I_{OH} = –4.0 mA
	High-drive output (P00, P01, P10, P11, P20 to P24, P27, P30 to P33, P70 to P76, P80 to P82, P90 to P96, PA0 to PA5, PB0, PB3 to PB7, PD0 to PD7, PE0, PE1, PE3 to PE5, and PN6)		—	4.98	—		I_{OH} = –0.5 mA
			—	4.97	—		I_{OH} = –1.0 mA
			—	4.94	—		I_{OH} = –2.0 mA
			—	4.87	—		I_{OH} = –4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	4.99	—		I_{OH} = –0.5 mA
			—	4.98	—		I_{OH} = –1.0 mA
			—	4.96	—		I_{OH} = –2.0 mA
			—	4.92	—		I_{OH} = –4.0 mA
			—	4.91	—		I_{OH} = –5.0 mA
Output low voltage	Normal drive output (all output pins)	V_{OL}	—	0.02	—	V	I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.09	—		I_{OL} = 2.0 mA
			—	0.18	—		I_{OL} = 4.0 mA
	High-drive output (P00, P01, P10, P11, P20 to P24, P27, P30 to P33, P70 to P76, P80 to P82, P90 to P96, PA0 to PA5, PB0, PB3 to PB7, PD0 to PD7, PE0, PE1, PE3 to PE5, and PN6)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.05	—		I_{OL} = 2.0 mA
			—	0.10	—		I_{OL} = 4.0 mA
			—	0.42	—		I_{OL} = 15.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.04	—		I_{OL} = 2.0 mA
			—	0.07	—		I_{OL} = 4.0 mA
			—	0.09	—		I_{OL} = 5.0 mA
			—	0.18	—		I_{OL} = 10.0 mA
			—	0.28	—		I_{OL} = 15.0 mA

Table 2.12 Standard Output Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = AVCC2 = 3.3 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Normal drive output (all output pins)	V_{OH}	—	3.26	—	V	I_{OH} = –0.5 mA
			—	3.22	—		I_{OH} = –1.0 mA
			—	3.13	—		I_{OH} = –2.0 mA
			—	2.94	—		I_{OH} = –4.0 mA
	High-drive output (P00, P01, P10, P11, P20 to P24, P27, P30 to P33, P70 to P76, P80 to P82, P90 to P96, PA0 to PA5, PB0, PB3 to PB7, PD0 to PD7, PE0, PE1, PE3 to PE5, and PN6)		—	3.28	—		I_{OH} = –0.5 mA
			—	3.26	—		I_{OH} = –1.0 mA
			—	3.22	—		I_{OH} = –2.0 mA
			—	3.13	—		I_{OH} = –4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	3.29	—		I_{OH} = –0.5 mA
			—	3.27	—		I_{OH} = –1.0 mA
			—	3.25	—		I_{OH} = –2.0 mA
			—	3.20	—		I_{OH} = –4.0 mA
			—	3.17	—		I_{OH} = –5.0 mA
Output low voltage	Normal drive output (all output pins)	V_{OL}	—	0.03	—	V	I_{OL} = 0.5 mA
			—	0.06	—		I_{OL} = 1.0 mA
			—	0.12	—		I_{OL} = 2.0 mA
			—	0.25	—		I_{OL} = 4.0 mA
	High-drive output (P00, P01, P10, P11, P20 to P24, P27, P30 to P33, P70 to P76, P80 to P82, P90 to P96, PA0 to PA5, PB0, PB3 to PB7, PD0 to PD7, PE0, PE1, PE3 to PE5, and PN6)		—	0.02	—		I_{OL} = 0.5 mA
			—	0.03	—		I_{OL} = 1.0 mA
			—	0.07	—		I_{OL} = 2.0 mA
			—	0.13	—		I_{OL} = 4.0 mA
	Large current output (P71 to P76, P81, P90 to P95, PB5, PD3)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.05	—		I_{OL} = 2.0 mA
			—	0.09	—		I_{OL} = 4.0 mA
			—	0.11	—		I_{OL} = 5.0 mA
			—	0.24	—		I_{OL} = 10.0 mA
			—	0.36	—		I_{OL} = 15.0 mA

Table 2.13 Thermal Resistance Value (Reference)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Package	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal resistance	100-pin LFQFP (PLQP0100KB-B)	θ_{ja}	—	—	50.5	°C/W	JESD51-2 and JESD51-7 compliant
	80-pin LFQFP (PLQP0080KB-B)		—	—	47.7		
	64-pin LFQFP (PLQP0064KB-C)		—	—	51.9		
	64-pin HWQFN (PWQN0064KF-A)		—	—	18.4*1		
	48-pin LFQFP (PLQP0048KB-B)		—	—	60.8		
	48-pin HWQFN (PWQN0048KC-A)		—	—	19.5*1		
	100-pin LFQFP (PLQP0100KB-B)	Ψ_{jt}	—	—	1.39	°C/W	JESD51-2 and JESD51-7 compliant
	80-pin LFQFP (PLQP0080KB-B)		—	—	1.39		
	64-pin LFQFP (PLQP0064KB-C)		—	—	1.88		
	64-pin HWQFN (PWQN0064KF-A)		—	—	0.12*1		
	48-pin LFQFP (PLQP0048KB-B)		—	—	2.38		
	48-pin HWQFN (PWQN0048KC-A)		—	—	0.12*1		

Note: The values are reference values when the 4-layer printed circuit board is used. Thermal resistance depends on the number of layers and size of the board. For details, refer to the JEDEC standards.

Note 1. The listed value applies when the exposed die pad is connected to VSS.

2.4 AC Characteristics

Table 2.14 Operating Frequency

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
System clock (ICLK)	f	—	—	120	MHz	
Peripheral module clock (PCLKA)		—	—	120		
Peripheral module clock (PCLKB)		—	—	60		
Peripheral module clock (PCLKC)		—	—	120		
Peripheral module clock (PCLKD)		8*1	—	60		AVCC0 = AVCC1 = AVCC2 ≥ 4.5 V
		8*1	—	40		AVCC0 = AVCC1 = AVCC2 < 4.5 V
Flash-IF clock (FCLK)		4*2	—	60		

Note 1. This restriction is only applied when a 12-bit A/D converter is to be used.
Note 2. This restriction is only applied when flash memory is to be programmed or erased.

2.4.1 Reset Timing

Table 2.15 Reset Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	2.0	—	—	ms	Figure 2.2
	Software standby mode	t_{RESWS}	0.3	—	—		Figure 2.3
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—		
Waiting time after release from the RES# pin reset		t_{RESWT}	70	—	71	t_{Lcyc}	Figure 2.2
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	116	—	124	t_{Lcyc}	

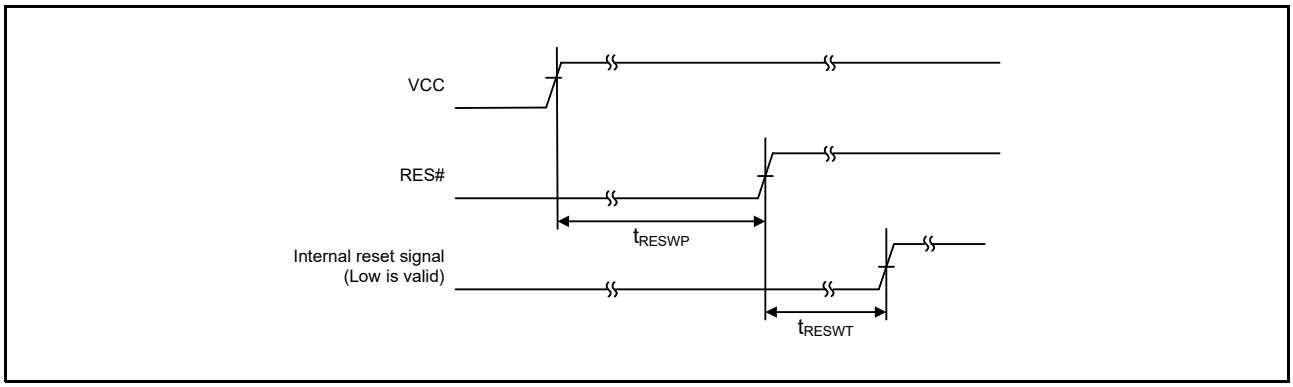


Figure 2.2 Reset Input Timing at Power-On

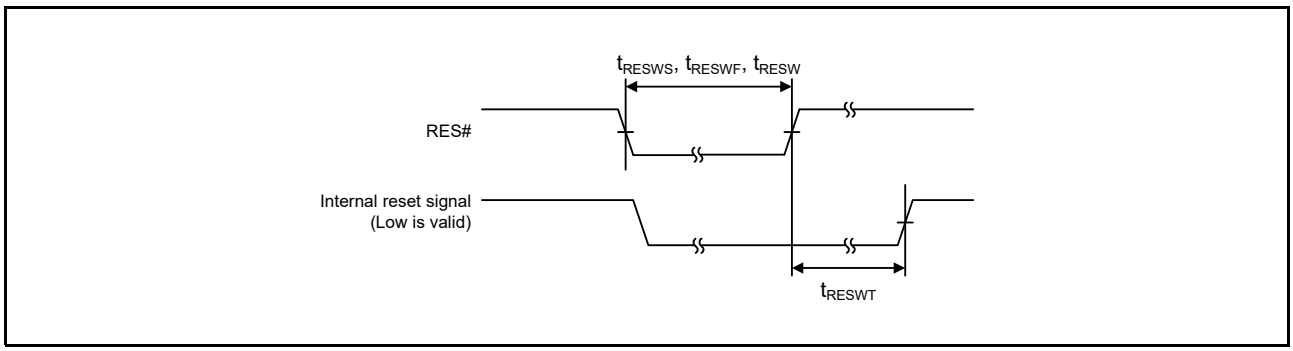


Figure 2.3 Reset Input Timing

2.4.2 Clock Timing

Table 2.16 EXTAL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 2.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

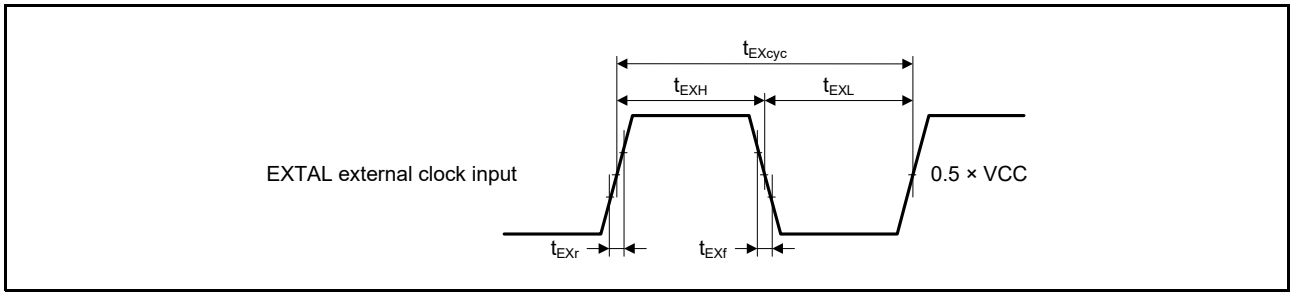


Figure 2.4 EXTAL External Clock Input Timing

Table 2.17 Main Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 2.5
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT} = [(MSTS[7:0] \text{ bits} \times 32) + 7] / f_{LOCO}$

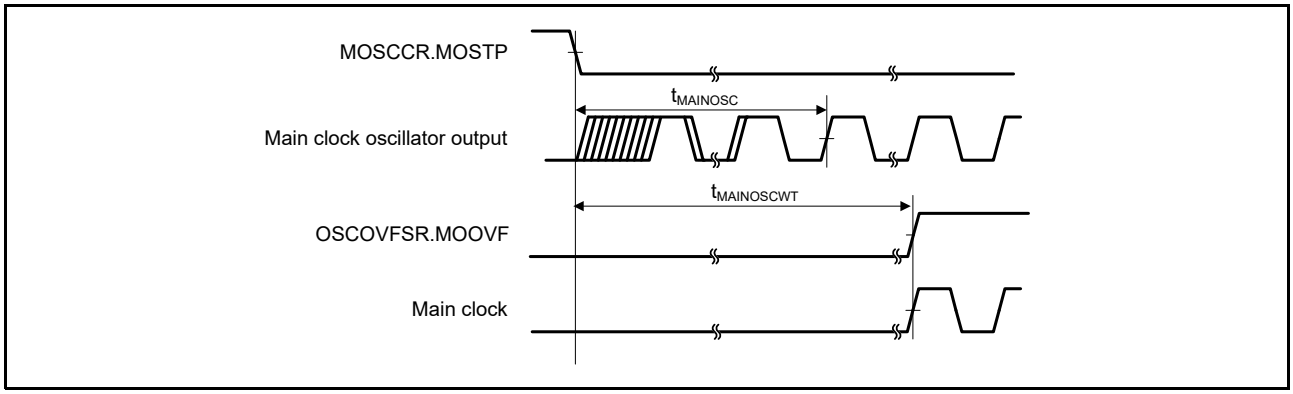


Figure 2.5 Main Clock Oscillation Start Timing

Table 2.18 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	3.78	4.16	4.63	µs	
LOCO clock oscillation frequency	f_{LOCO}	216 (–10%)	240	264 (+10%)	kHz	
LOCO clock oscillation stabilization time	t_{LOCOWT}	—	—	44	µs	Figure 2.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	7.57	8.33	9.26	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108 (–10%)	120	132 (+10%)	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 2.7

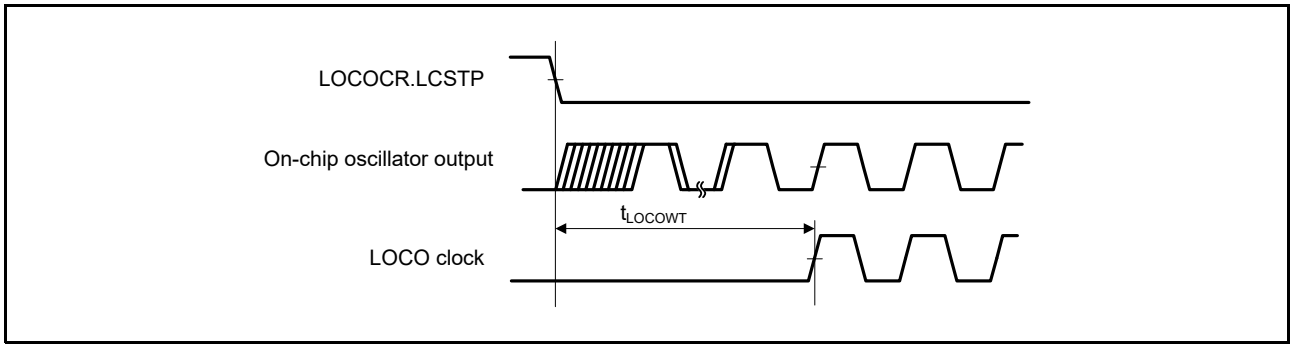


Figure 2.6 LOCO Clock Oscillation Start Timing

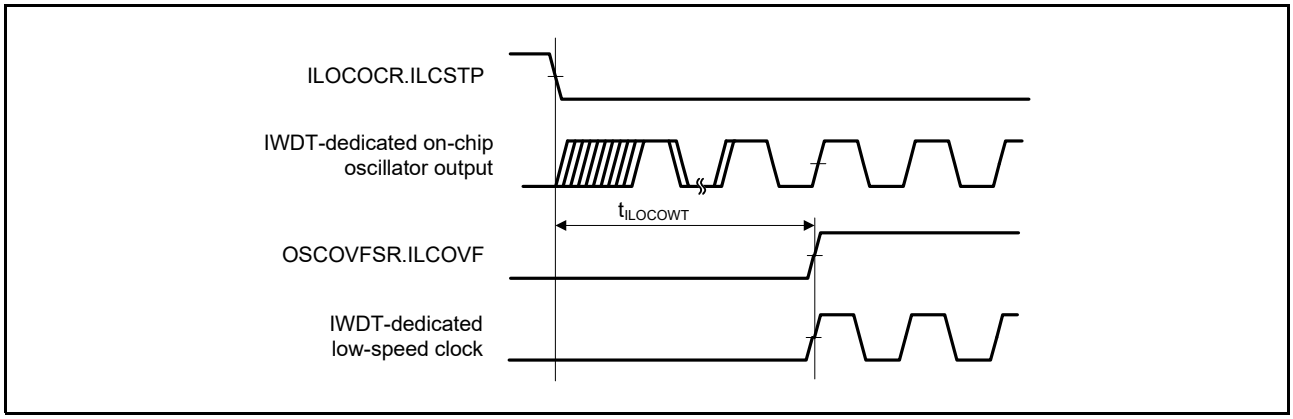


Figure 2.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 2.19 HOCO Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.84 (–1.0%)	16	16.16 (+1.0%)	MHz	–20°C ≤ T_a
		17.82 (–1.0%)	18	18.18 (+1.0%)		
		19.80 (–1.0%)	20	20.20 (+1.0%)		
		15.76 (–1.5%)	16	16.24 (+1.5%)		T_a < –20°C
		17.73 (–1.5%)	18	18.27 (+1.5%)		
		19.70 (–1.5%)	20	20.30 (+1.5%)		
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	μs	Figure 2.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	μs	Figure 2.9

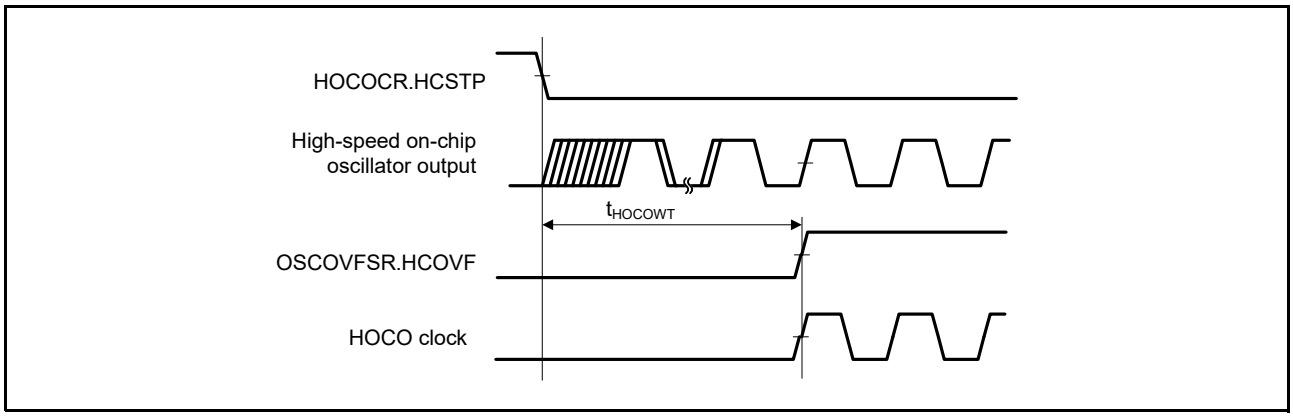


Figure 2.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

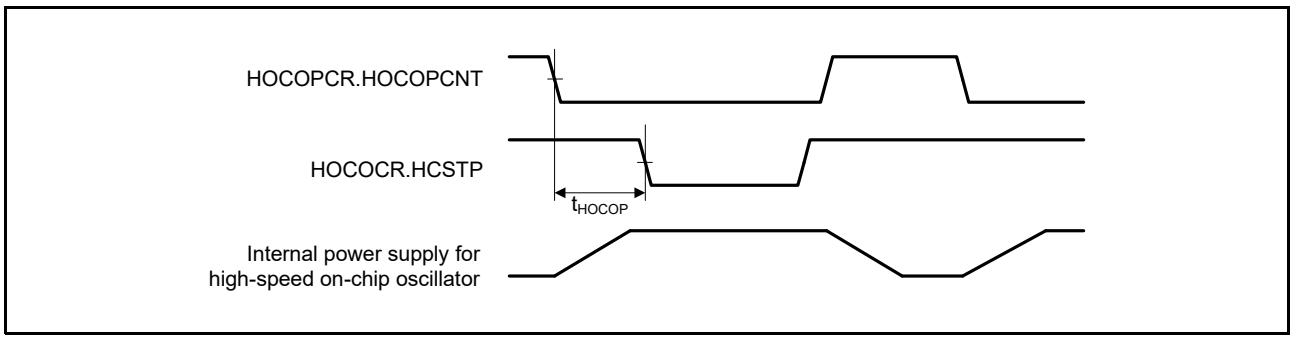


Figure 2.9 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 2.20 PLL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	µs	Figure 2.10

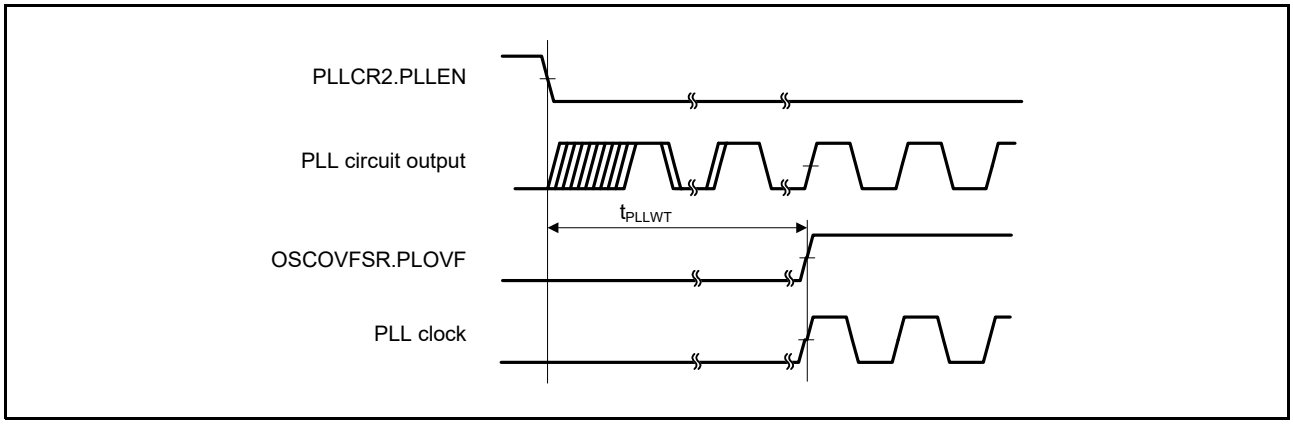


Figure 2.10 PLL Clock Oscillation Start Timing

2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.21 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time after cancellation of software standby mode*1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bits × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	µs	Figure 2.11
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	—	{(MSTS[7:0] bits × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	—	—	352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	—	—	639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}	—	—	454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}	µs	
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}	—	—	741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}	—	—	338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}	µs	

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK} : f_{FCLK}$ = 1 : 1, 2 : 1, or 4 : 1.

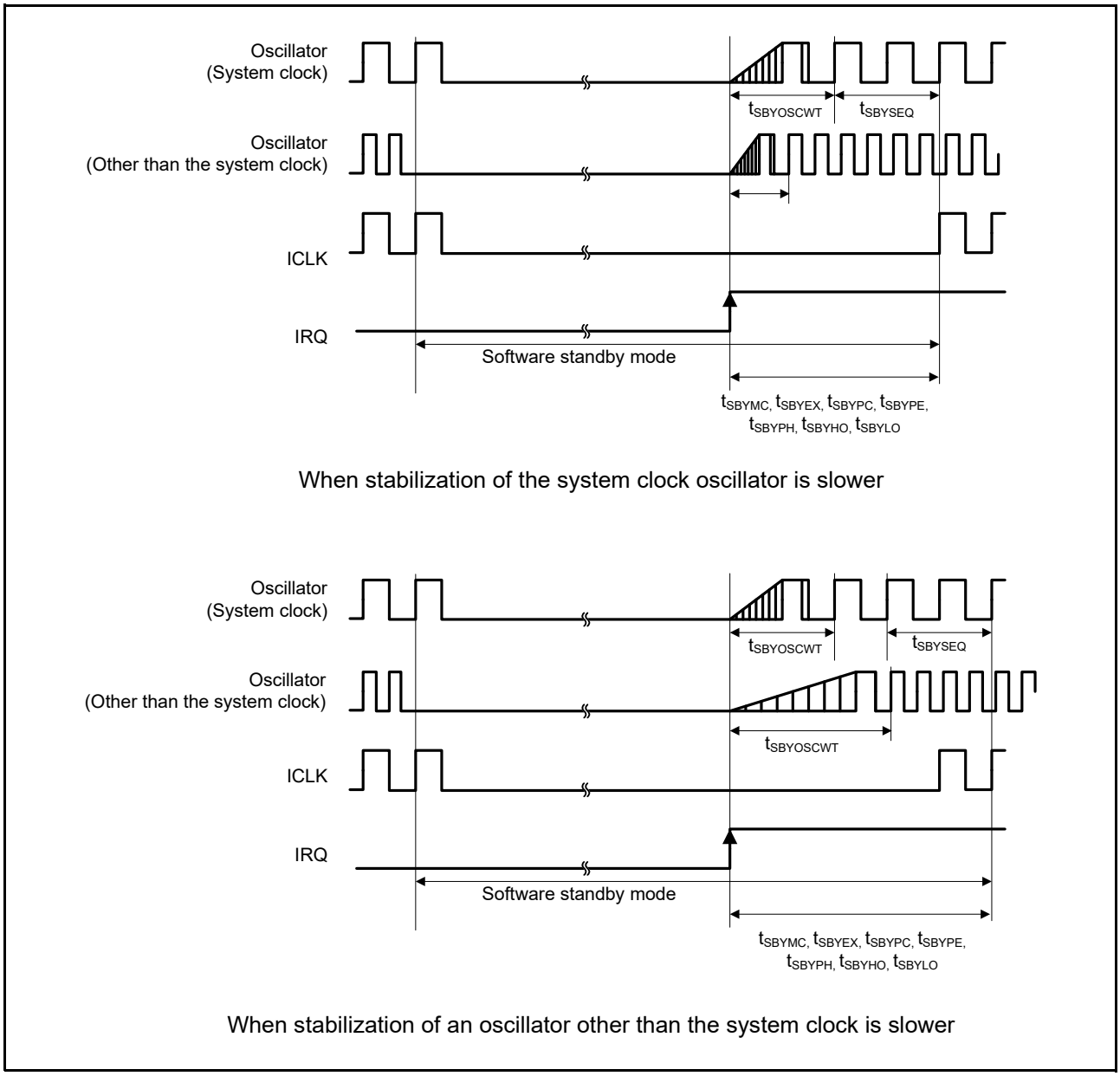


Figure 2.11 Software Standby Mode Cancellation Timing

2.4.4 Control Signal Timing

Table 2.22 Control Signal Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	$2 \times t_{PBcyc} \leq 200$ ns, Figure 2.12
		$2 \times t_{PBcyc}$	—	—		$2 \times t_{PBcyc} > 200$ ns, Figure 2.12
IRQ pulse width	t_{IRQW}	200	—	—	ns	$2 \times t_{PBcyc} \leq 200$ ns, Figure 2.13
		$2 \times t_{PBcyc}$	—	—		$2 \times t_{PBcyc} > 200$ ns, Figure 2.13

Note 1. t_{PBcyc}: PCLKB cycle

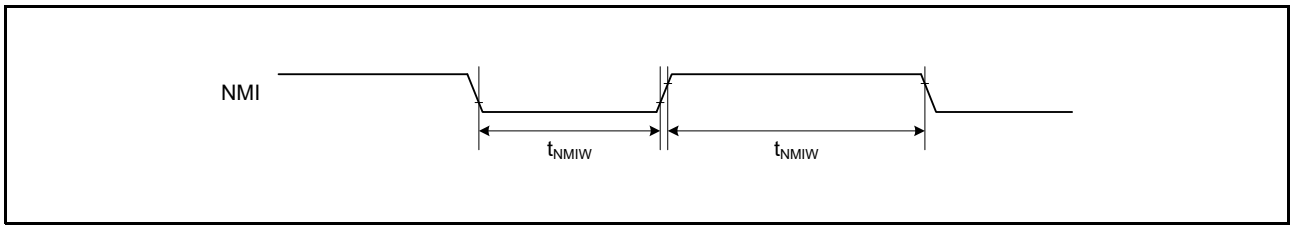


Figure 2.12 NMI Interrupt Input Timing

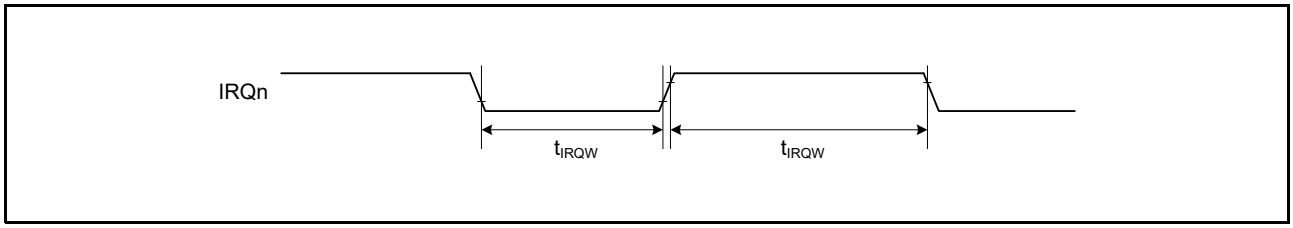


Figure 2.13 IRQ Interrupt Input Timing

2.4.5 Timing of On-Chip Peripheral Modules

2.4.5.1 I/O Port

Table 2.23 I/O Port Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.14

Note 1. t_{PBcyc}: PCLKB cycle

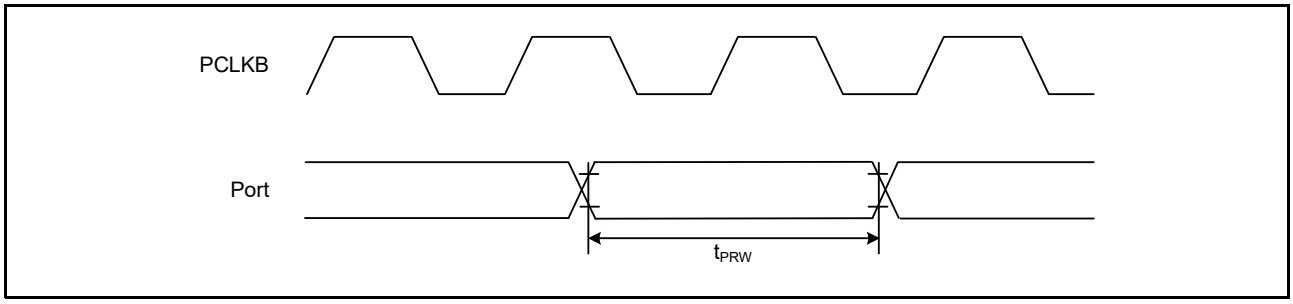


Figure 2.14 I/O Port Input Timing

2.4.5.2 TMR

Table 2.24 TMR Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.15
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

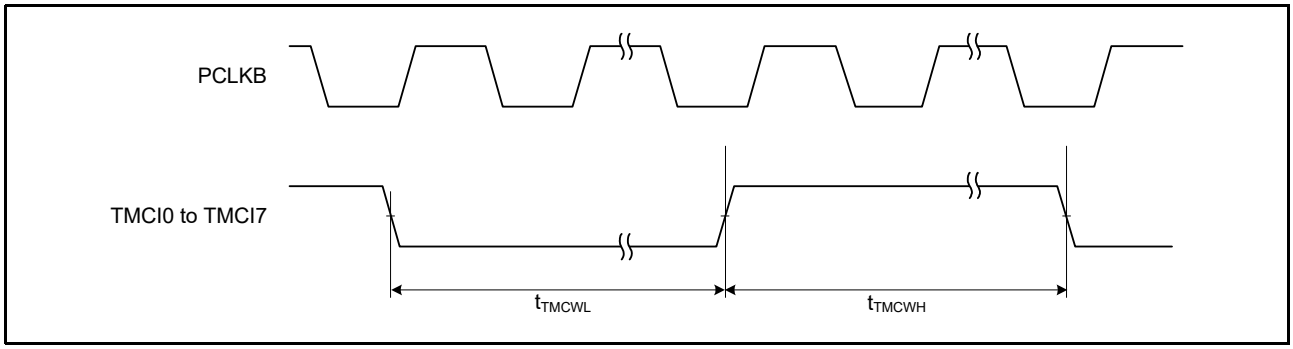


Figure 2.15 TMR Clock Input Timing

2.4.5.3 MTU

Table 2.25 MTU Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PCcyc}	Figure 2.16
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PCcyc}	Figure 2.17
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PCcyc}: PCLKC cycle

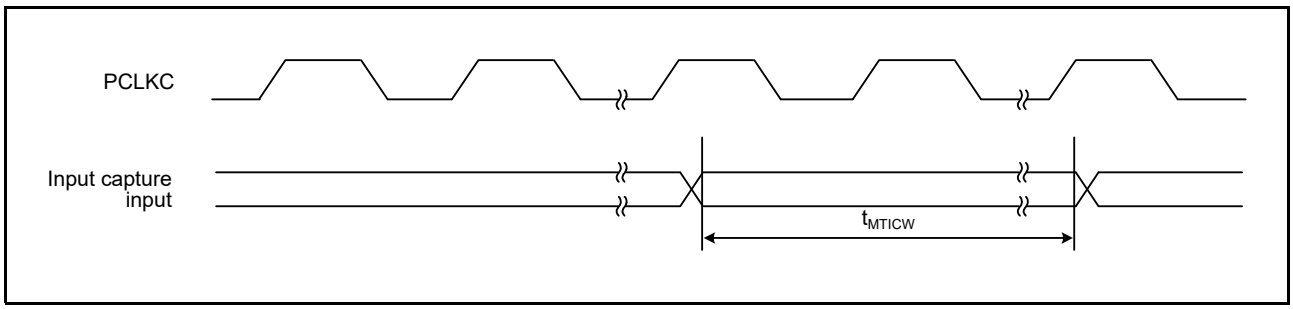


Figure 2.16 MTU Input Capture Input Timing

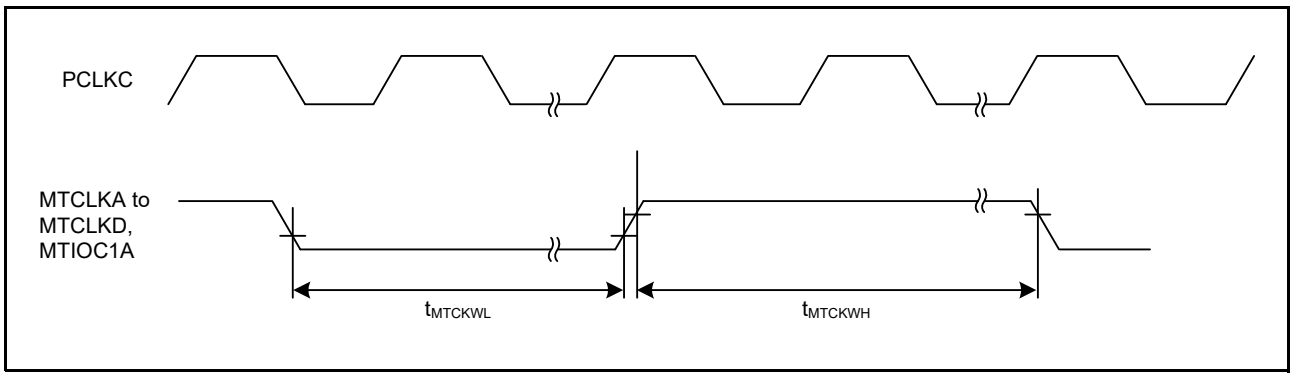


Figure 2.17 MTU Clock Input Timing

2.4.5.4 POE3

Table 2.26 POE3 Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, and 8 to 12)		t_{POEW}	1.5	—	—	t_{PBcyc}	Figure 2.18
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.19 When detecting falling edges (ICSRm.POEnM[3:0] = 0000 (m = 1 to 8, n = 0, 4, 8 to 12))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.20
		Detection of comparator outputs	t_{POEDC}	—	—	5 PCLKB + 0.2	µs	Figure 2.21 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C.
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.22 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.23

Note 1. t_{PBcyc}: PCLKB cycle

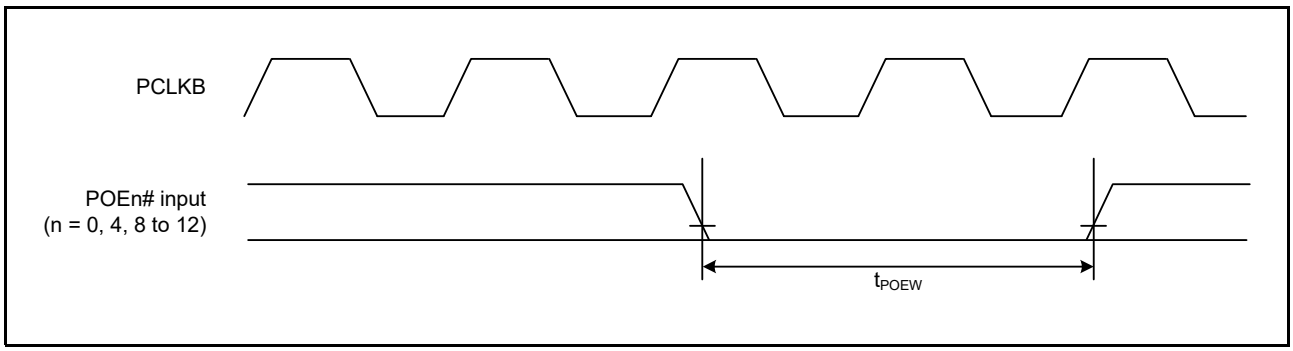


Figure 2.18 POE Input Timing

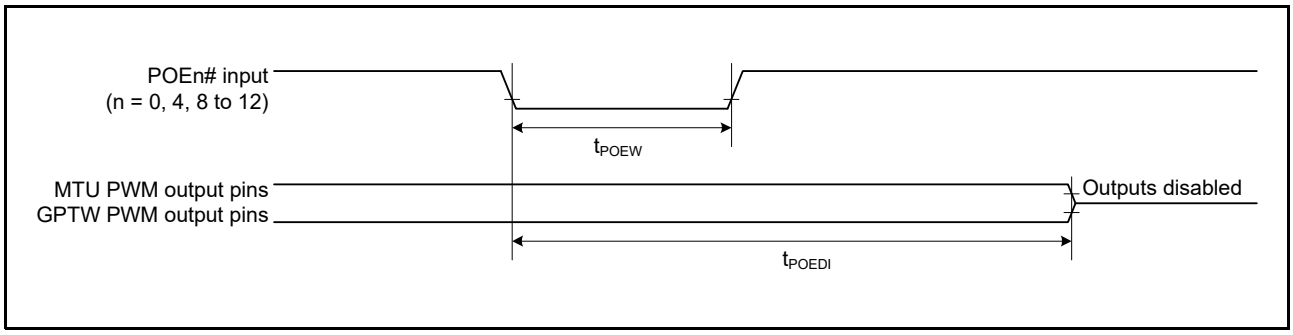
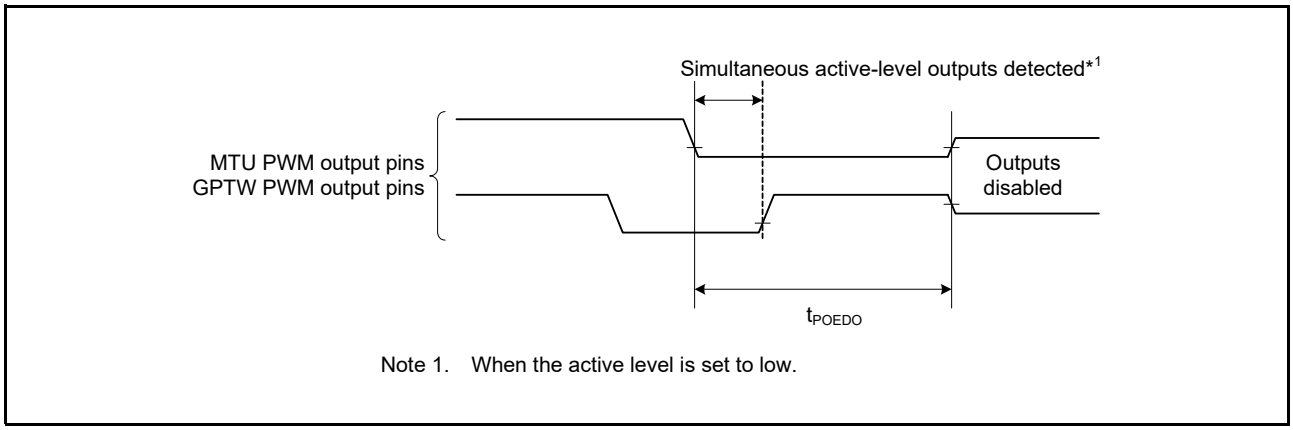


Figure 2.19 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.20 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

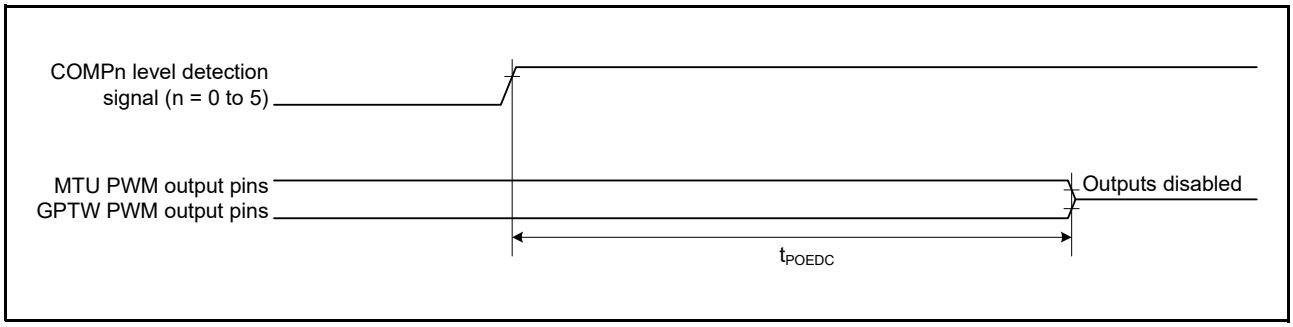


Figure 2.21 Output Disable Time for POE in Response to Detection of the Comparator Outputs

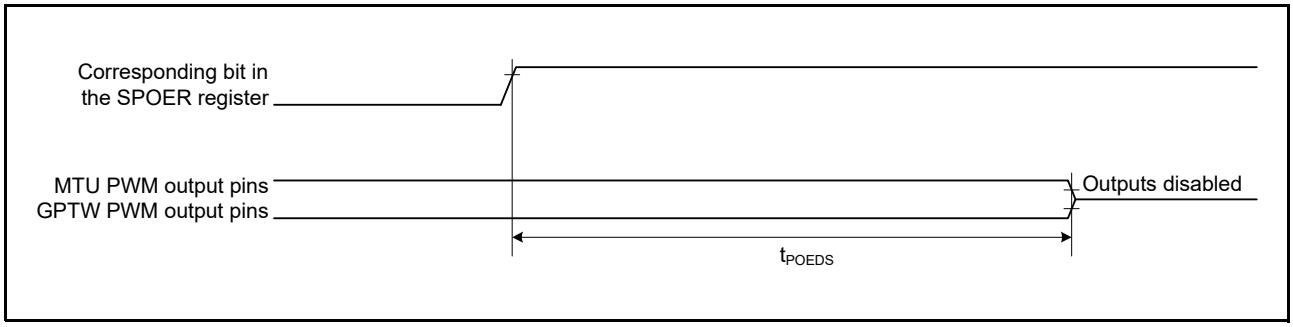


Figure 2.22 Output Disable Time for POE in Response to the Register Setting

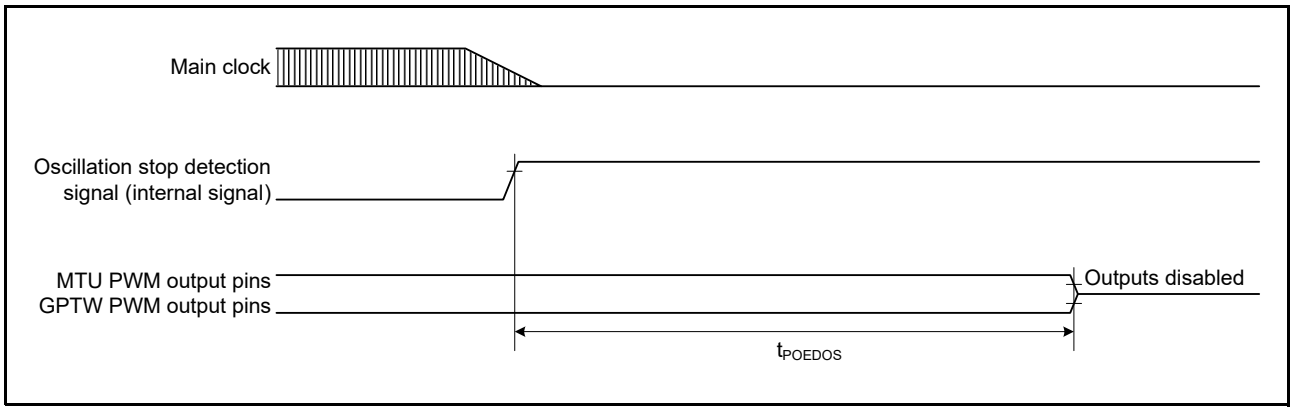


Figure 2.23 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.4.5.5 POEG

Table 2.27 POE and POEG Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	1.5	—	—	t_{PBcyc}	Figure 2.24
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	—	3 PCLKB + 0.34	µs	Figure 2.25 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	—	0.5	µs	Figure 2.26
		Edge detection signal from a comparator	t_{POEGDC}	—	—	4 PCLKB + 0.5	µs	Figure 2.27 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C.
		Register setting	t_{POEGDS}	—	—	1 PCLKB + 0.3	µs	Figure 2.28 Time for access to the register is not included.
		Oscillation stop detection	$t_{POEGDOS}$	—	—	21	µs	Figure 2.29
		Input level detection of the GTETRGn pin (direct path)	$t_{POEGDDI}$	—	—	2 PCLKB + 1 PCLKC + 0.34	µs	Figure 2.30
		Level detection signal from a comparator	$t_{POEGDDC}$	—	—	3 PCLKB + 0.3	µs	Figure 2.31 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C.

Note 1. t_{PBcyc}: PCLKB cycle

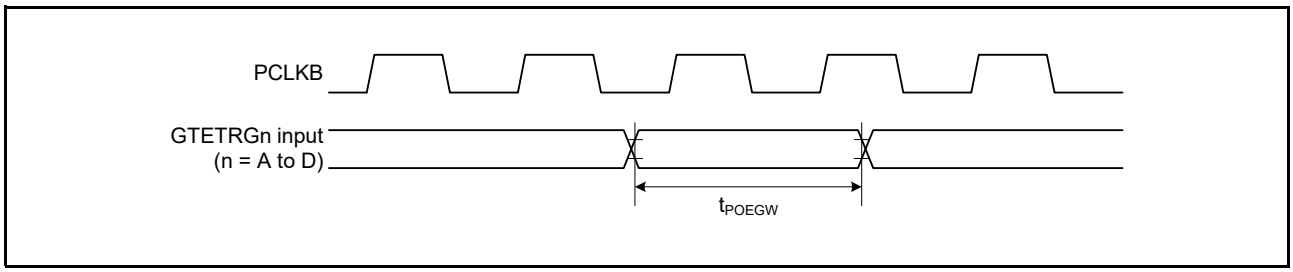


Figure 2.24 POEG Input Timing

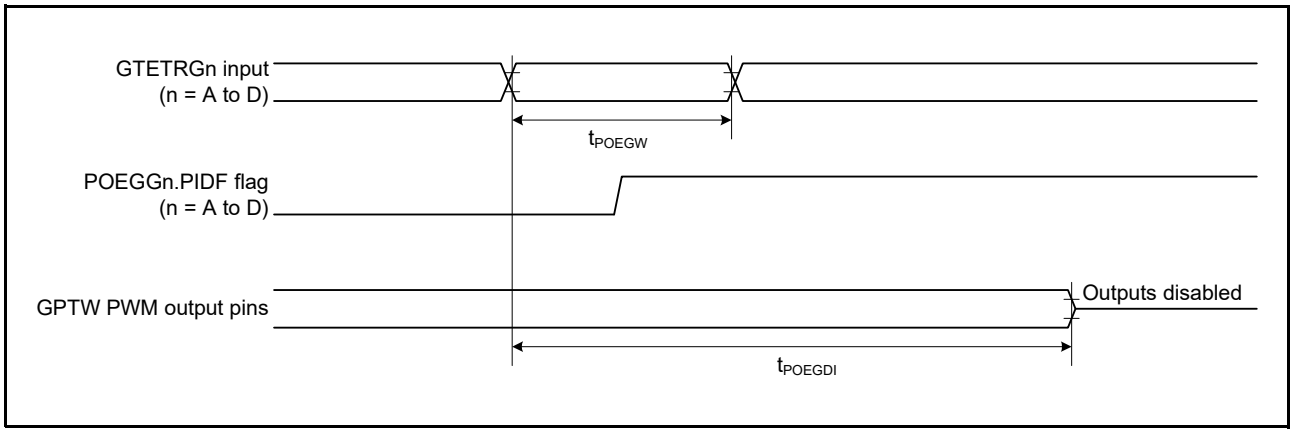
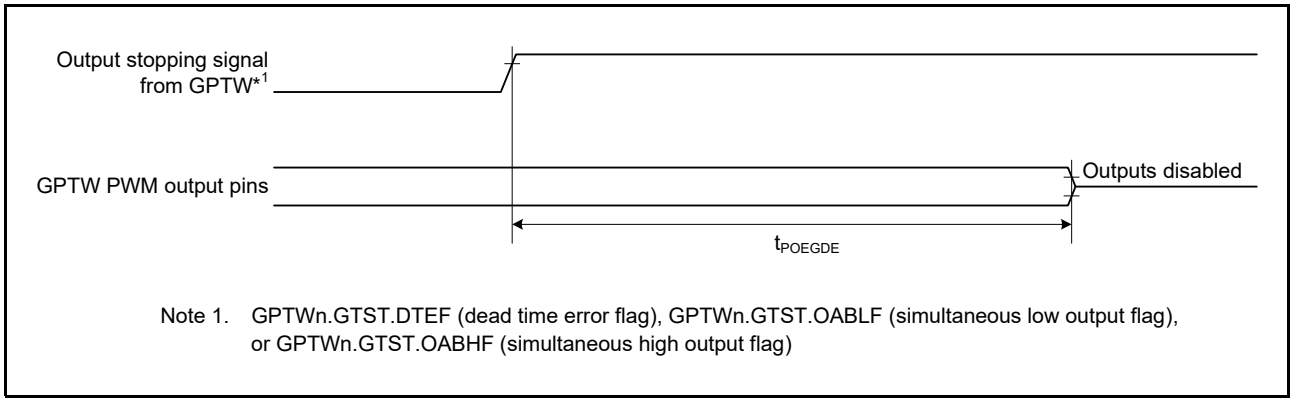


Figure 2.25 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin



Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

Figure 2.26 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

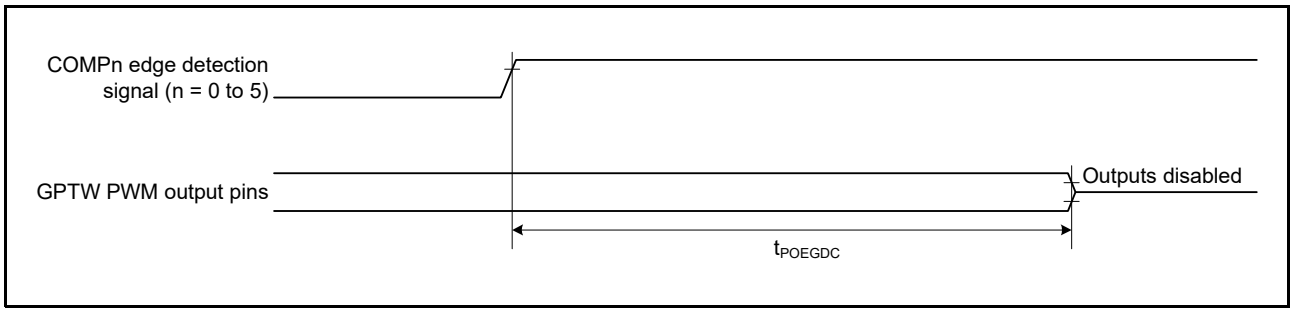


Figure 2.27 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

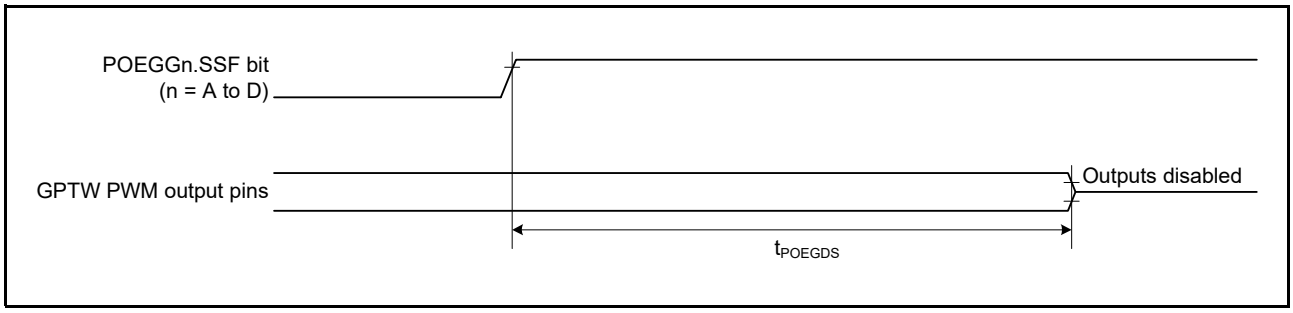


Figure 2.28 Output Disable Time for POEG in Response to the Register Setting

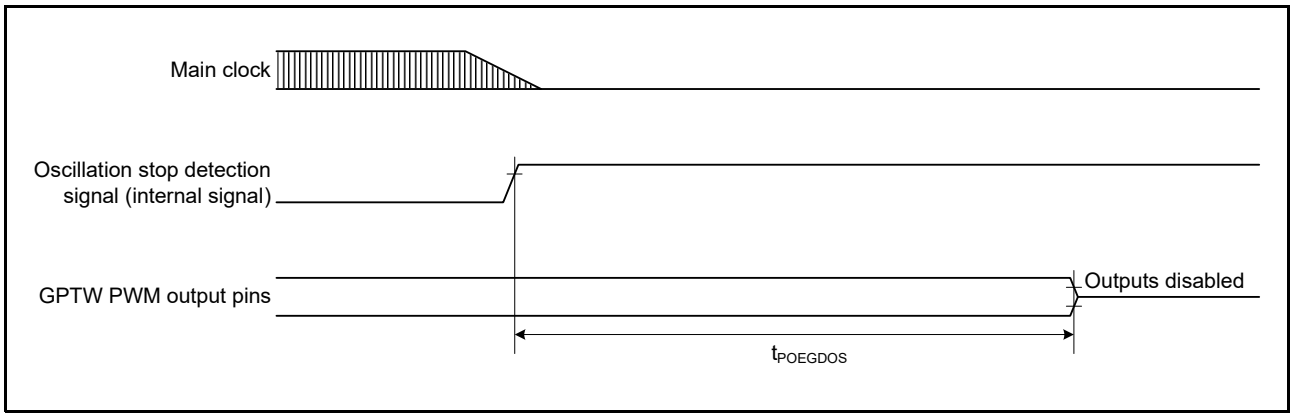


Figure 2.29 Output Disable Time of POEG in Response to the Oscillation Stop Detection

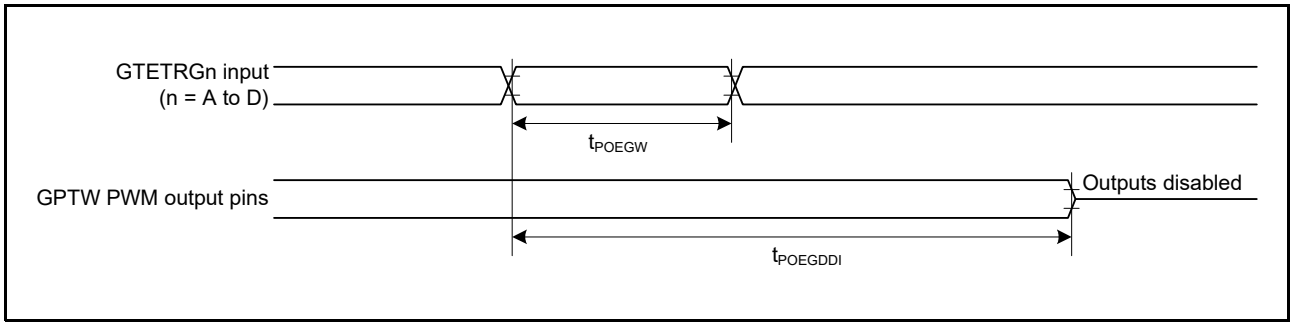


Figure 2.30 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRGn pin

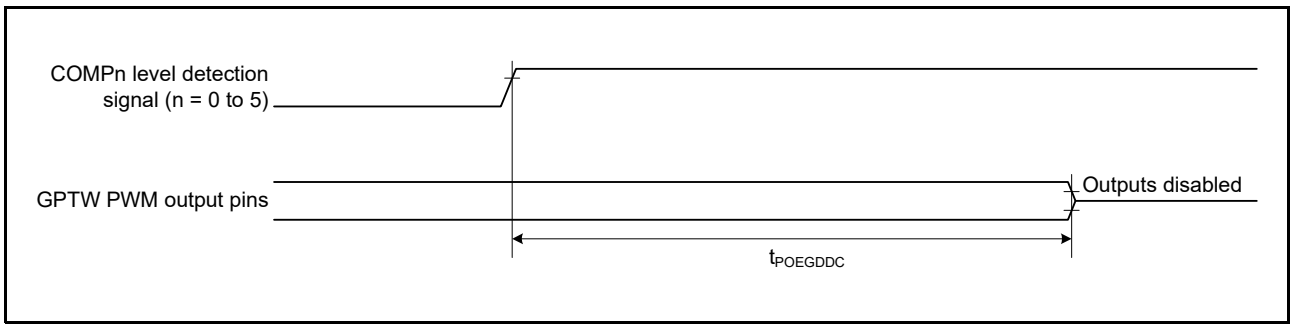


Figure 2.31 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator

2.4.5.6 GPTW

Table 2.28 GPTW Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1, *2	Test Conditions
GPTW	Input capture input pulse width	Single-edge setting	t_{GTICW}	1.5	—	t_{PCcyc}	Figure 2.32
		Both-edge setting		2.5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PBcyc}	Figure 2.33
		Both-edge setting		2.5	—		
	Timer clock pulse width		t_{GTCKWH}	1.5	—	t_{PBcyc}	Figure 2.34
			t_{GTCKWL}				

Note 1. t_{PCcyc}: PCLKC cycle
Note 2. t_{PBcyc}: PCLKB cycle

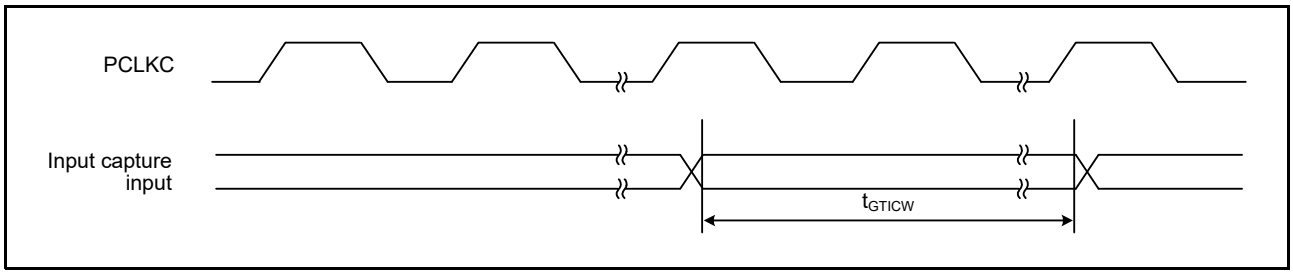


Figure 2.32 GPTW Input Capture Input Timing

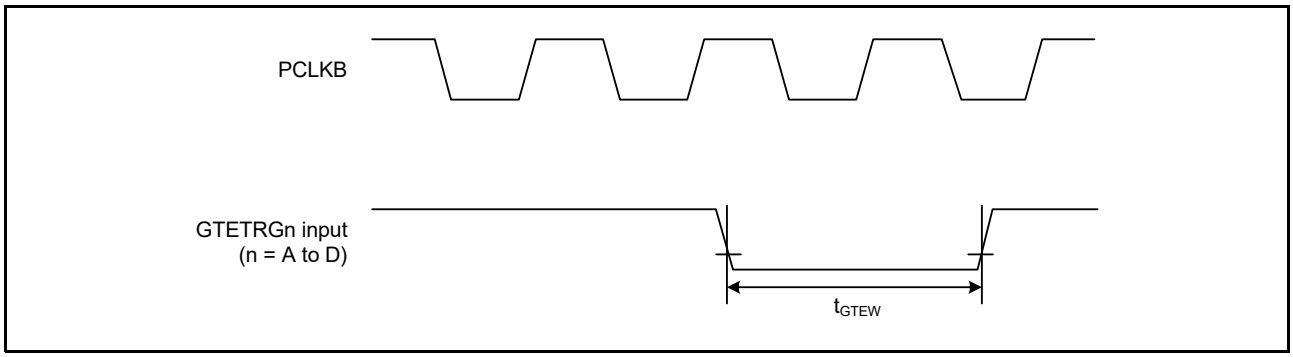


Figure 2.33 GPTW External Trigger Input Timing

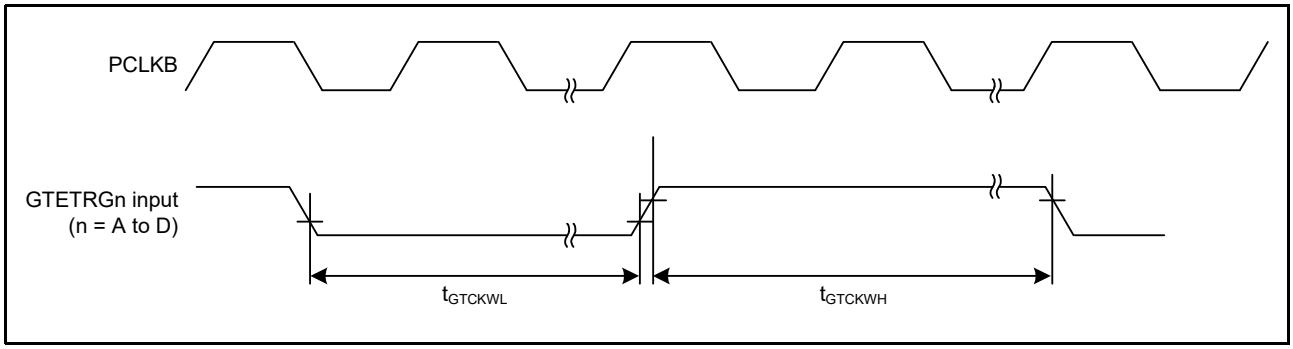


Figure 2.34 GPTW Clock Input Timing

2.4.5.7 A/D Converter Trigger

Table 2.29 A/D Converter Trigger Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.35

Note 1. t_{PBcyc}: PCLKB cycle

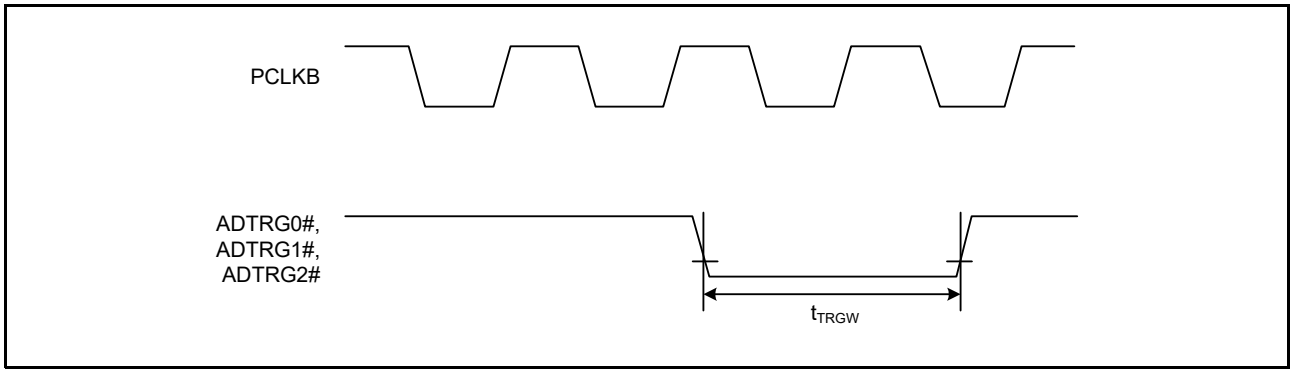


Figure 2.35 A/D Converter Trigger Input Timing

2.4.5.8 CAC

Table 2.30 CAC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item*1, *2			Symbol	Min.*1, *2	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$	t_{CACREF}	$4.5\ t_{cac} + 3\ t_{PBcyc}$	—	ns	
		$t_{PBcyc} > t_{cac}$		$5\ t_{cac} + 6.5\ t_{PBcyc}$	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

2.4.5.9 SCI

Table 2.31 SCIk and SCIh Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
SCIk, SCIh	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.36	
		Clock synchronous		6	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous (SCIk)	t_{Scyc}	6	—	t_{PBcyc}		
		Asynchronous (SCIh)		8	—			
		Clock synchronous		4	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	VCC ≥ 4.5 V	Figure 2.37
				—	33		VCC < 4.5 V	
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	Figure 2.37	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns		

Note 1. t_{PBcyc}: PCLKB cycle

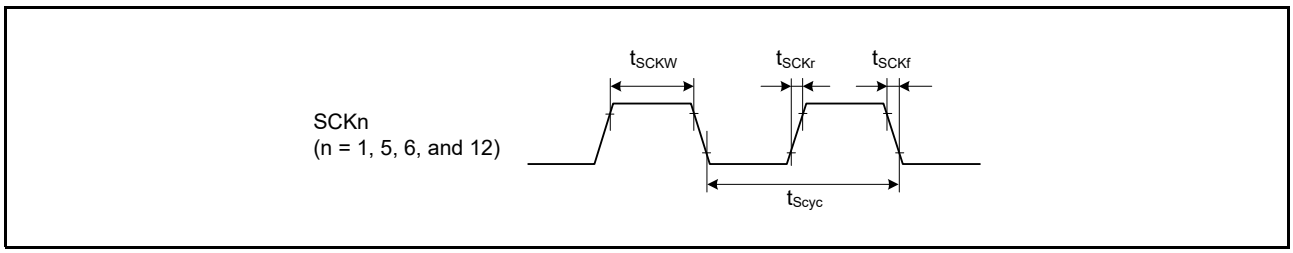


Figure 2.36 SCK Clock Input Timing

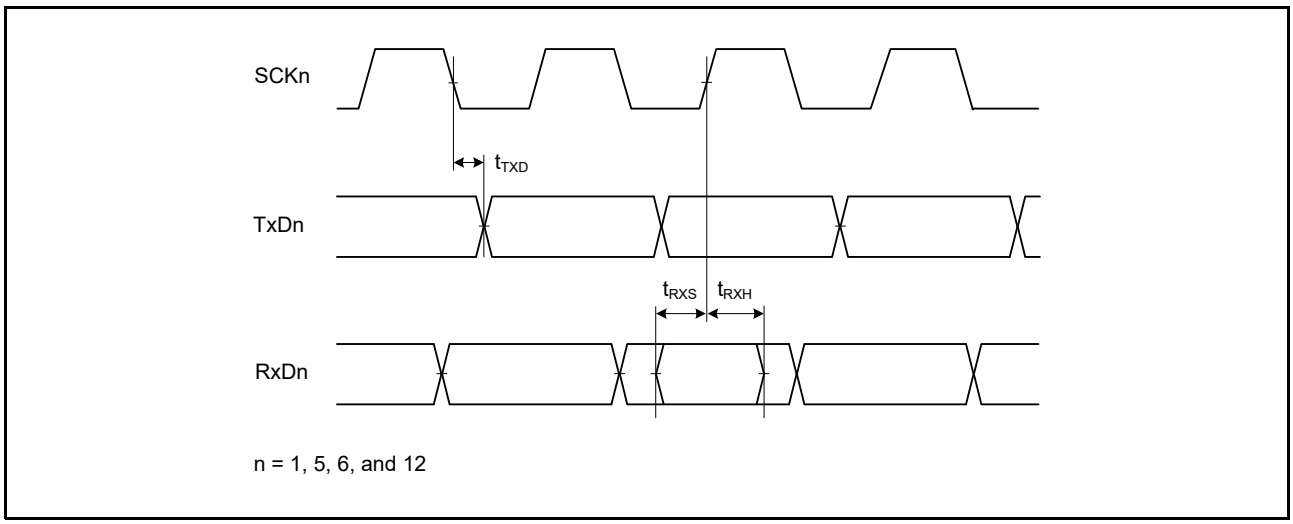


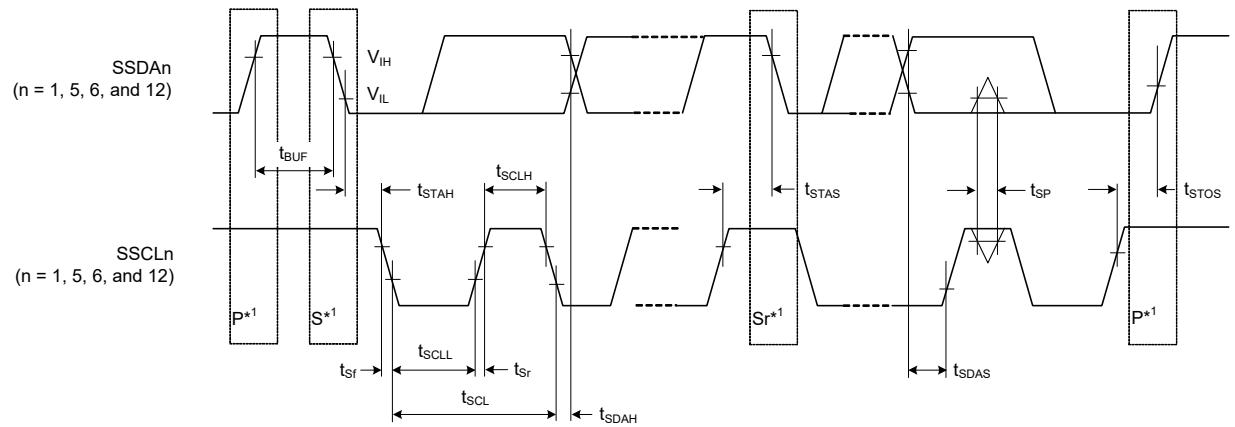
Figure 2.37 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.32 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.*1	Unit	Test Conditions
Simple IIC (Standard-mode)	SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.38
	SSDA input fall time	t_{Sf}	—	300		
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}		
	Data input setup time	t_{SDAS}	250	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL, SSDA capacitive load	C_b*2	—	400	pF	
Simple IIC (Fast-mode)	SSDA input rise time	t_{Sr}	—	300	ns	
	SSDA input fall time	t_{Sf}	—	300		
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}		
	Data input setup time	t_{SDAS}	100	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL, SSDA capacitive load	C_b*2	—	400	pF	

Note 1. t_{Pcyc} refers to the period of PCLKB.
Note 2. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA
V_{OL} = 0.4 V, I_{OL} = 3 mA

Figure 2.38 Simple IIC Bus Interface Input/Output Timing

Table 2.33 Simple SPI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	—	t_{Pcyc}	Figure 2.39
	SCK clock cycle input (slave)		6	—		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.40 to Figure 2.43
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 2.42, Figure 2.43
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc} refers to the period of PCLKB.

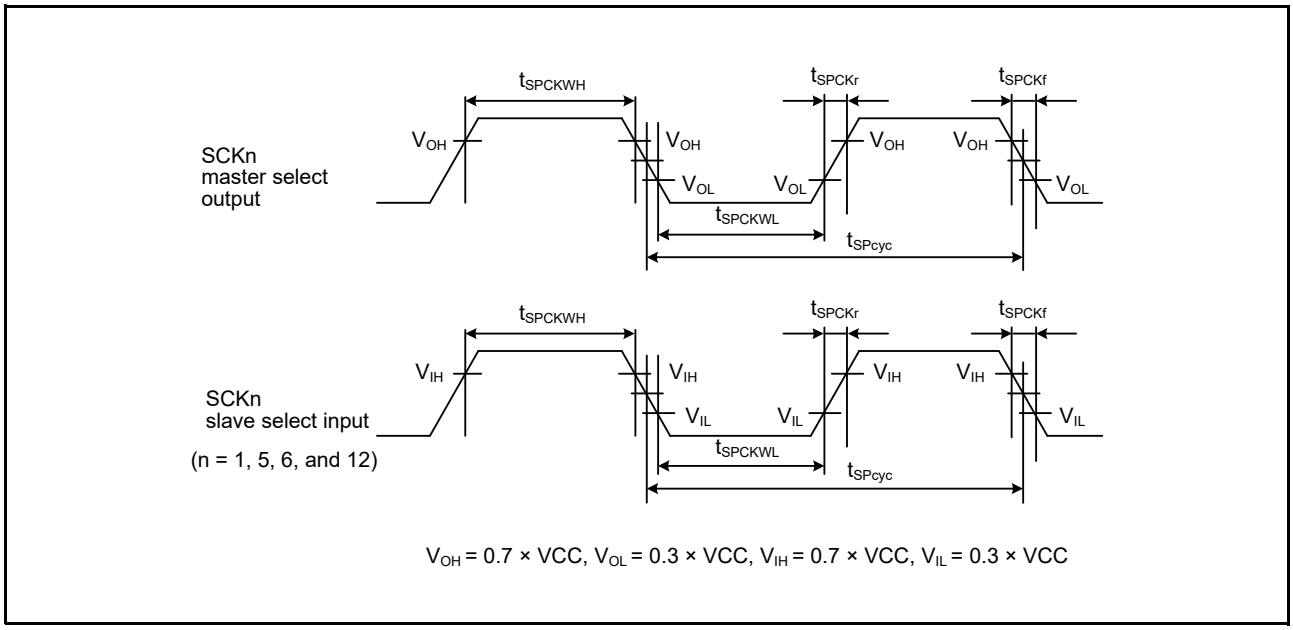


Figure 2.39 Simple SPI Clock Timing

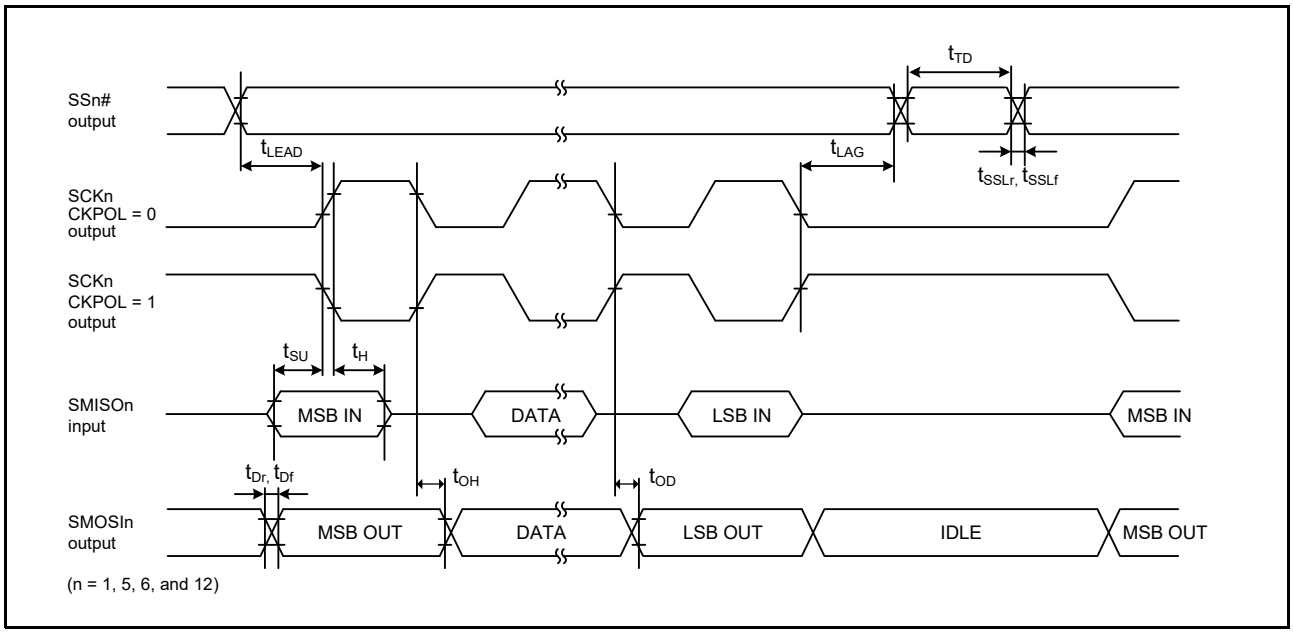


Figure 2.40 Simple SPI Timing (Master, CKPH = 1)

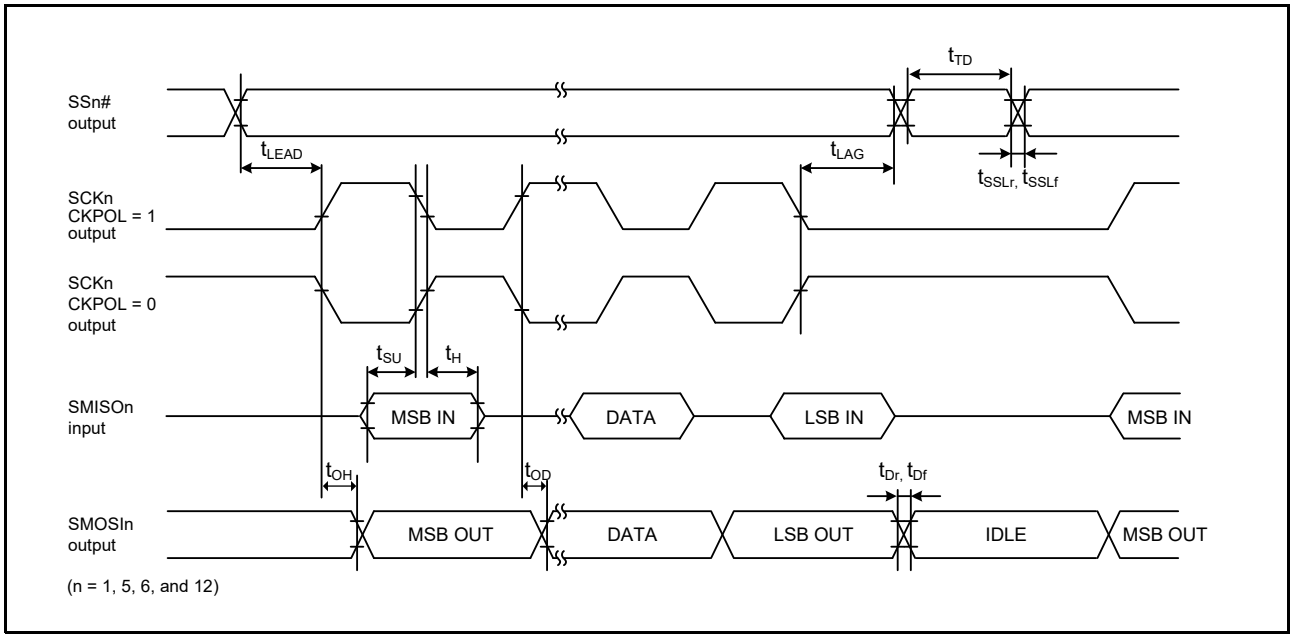


Figure 2.41 Simple SPI Timing (Master, CKPH = 0)

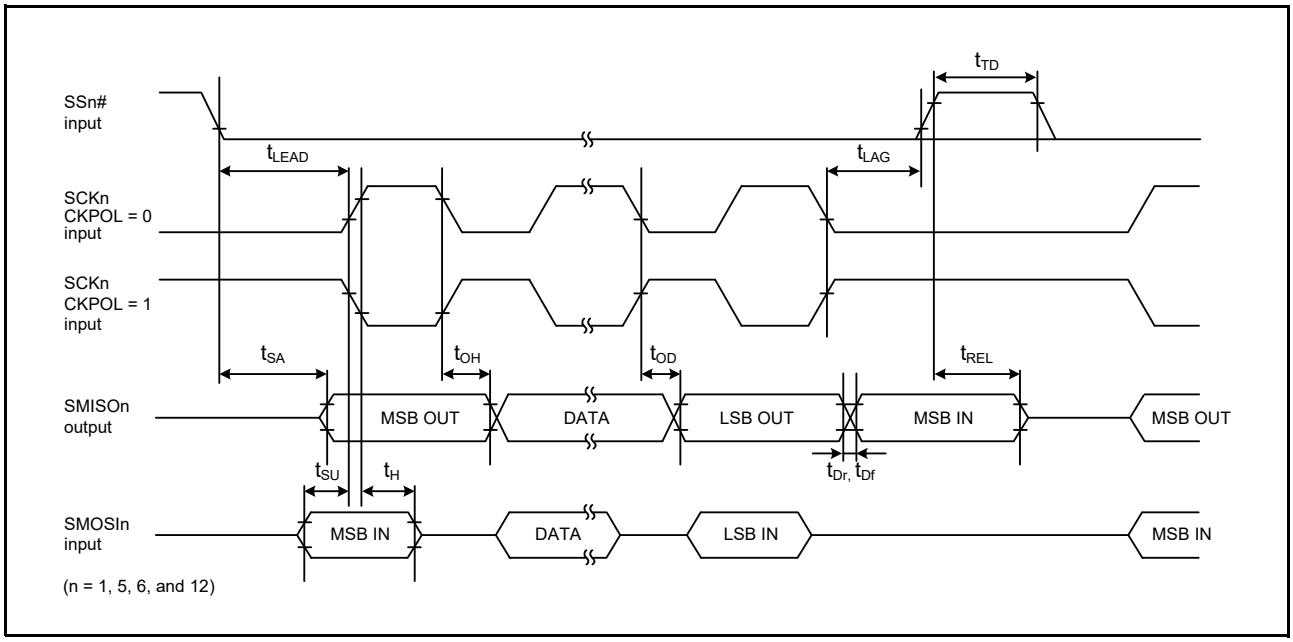


Figure 2.42 Simple SPI Timing (Slave, CKPH = 1)

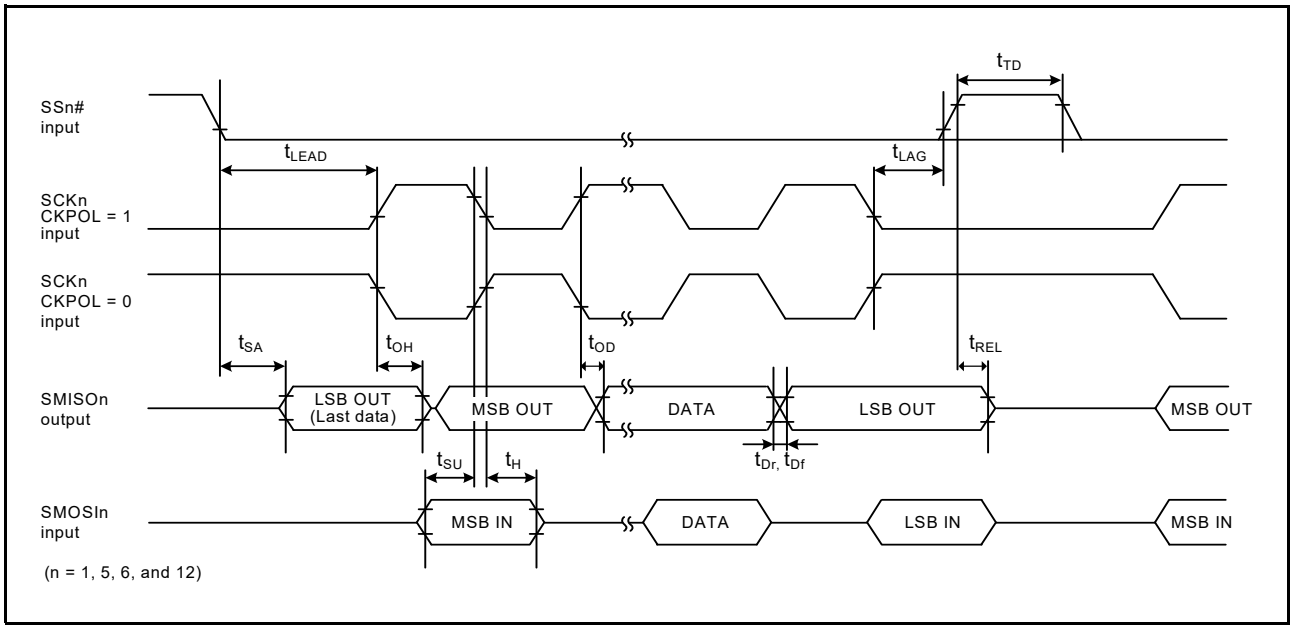


Figure 2.43 Simple SPI Timing (Slave, CKPH = 0)

2.4.5.10 RSCI

Table 2.34 RSCI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions	
RSCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.44	
		Clock synchronous		2	—			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	—	5	ns		
	Input clock fall time		t_{SCKf}	—	5	ns		
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}		
		Clock synchronous		2	—			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	—	5	ns		
	Output clock fall time		t_{SCKf}	—	5	ns		
	Receive data setup time	Master	t_{RXS}	–1.5	—	ns	VCC ≥ 4.5 V	Figure 2.45
				3.5	—		VCC < 4.5 V	
		Slave		2.5	—		Figure 2.45	
	Receive data hold time	Master	t_{RXH}	11	—	ns		
		Slave		2.5	—			
	Transmit data delay time	Master	t_{TXD}	—	4	ns		
		Slave		—	17		VCC ≥ 4.5 V	Figure 2.45
				—	22		VCC < 4.5 V	

Note 1. t_{Pcyc} refers to the period of PCLKB in RSCI8 and RSCI9, and of PCLKA in RSCI11.

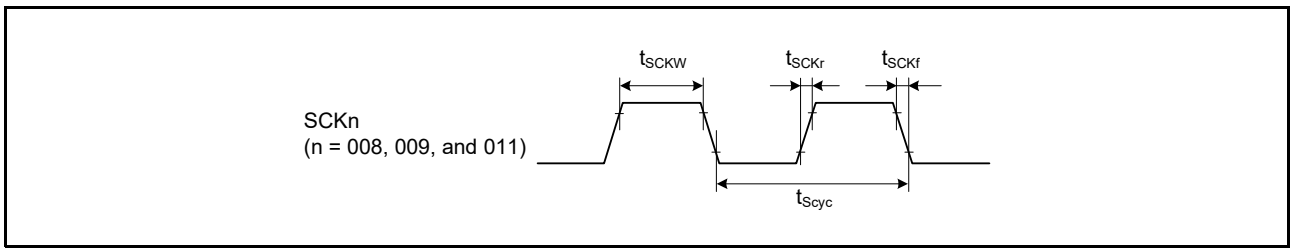


Figure 2.44 SCK Clock Input Timing

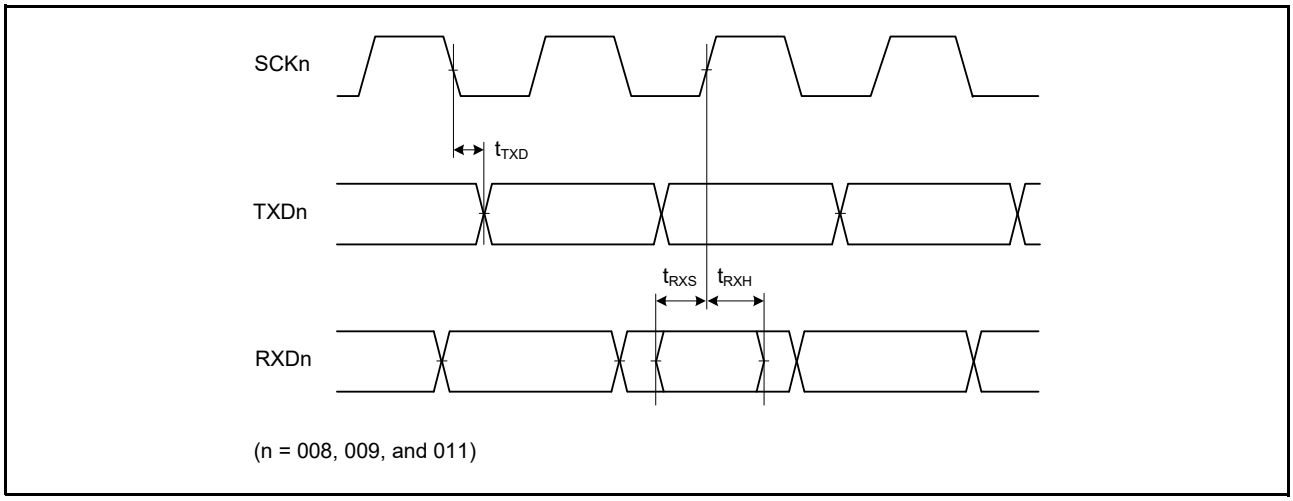


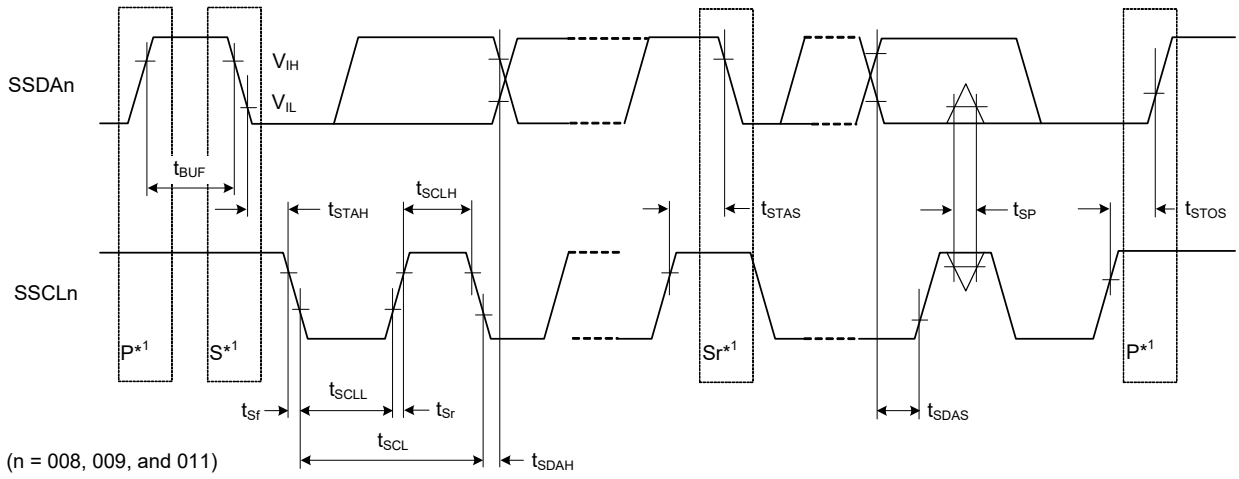
Figure 2.45 RSCI Input/Output Timing: Clock Synchronous Mode

Table 2.35 Simple IIC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.46
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc} refers to the period of PCLKB in RSCI8 and RSCI9, and of PCLKA in RSCI11.
Note 1. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA

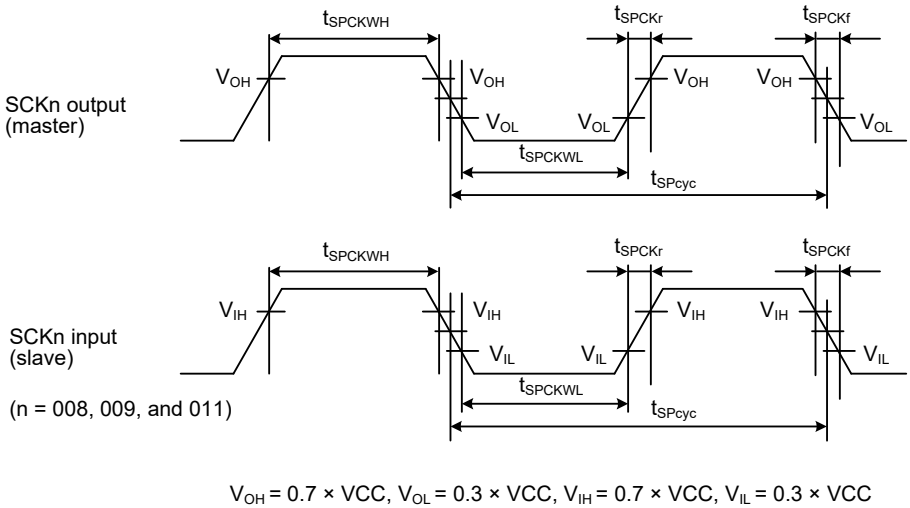
Figure 2.46 Simple IIC Bus Interface Input/Output Timing

Table 2.36 Simple SPI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	2	—	t_{Pcyc}	Figure 2.47
	SCK clock cycle input (slave)			2	—		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input		—	1	μs	
	Data input setup time	Master	t_{SU}	0.5	—	ns	Figure 2.48 to Figure 2.51
		Slave		2.5	—		
	Data input hold time	Master	t_H	11	—	ns	
		Slave		2.5	—		
	Data output delay time	Master	t_{OD}	—	4	ns	Figure 2.48 to Figure 2.51
		Slave		—	17		VCC ≥ 4.5V: Figure 2.48 to Figure 2.51
				—	22		VCC < 4.5V: Figure 2.48 to Figure 2.51
	Data output hold time	Master	t_{OH}	–1	—	ns	Figure 2.48 to Figure 2.51
		Slave		0	—		
	Data rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	—	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	Figure 2.50, Figure 2.51
	Slave output release time		t_{REL}	—	5	t_{Pcyc}	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	Figure 2.48 to Figure 2.51
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	1	μs	

Note 1. t_{Pcyc} refers to the period of PCLKB in RSCI8 and RSCI9, and of PCLKA in RSCI11.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.47 Simple SPI Clock Timing

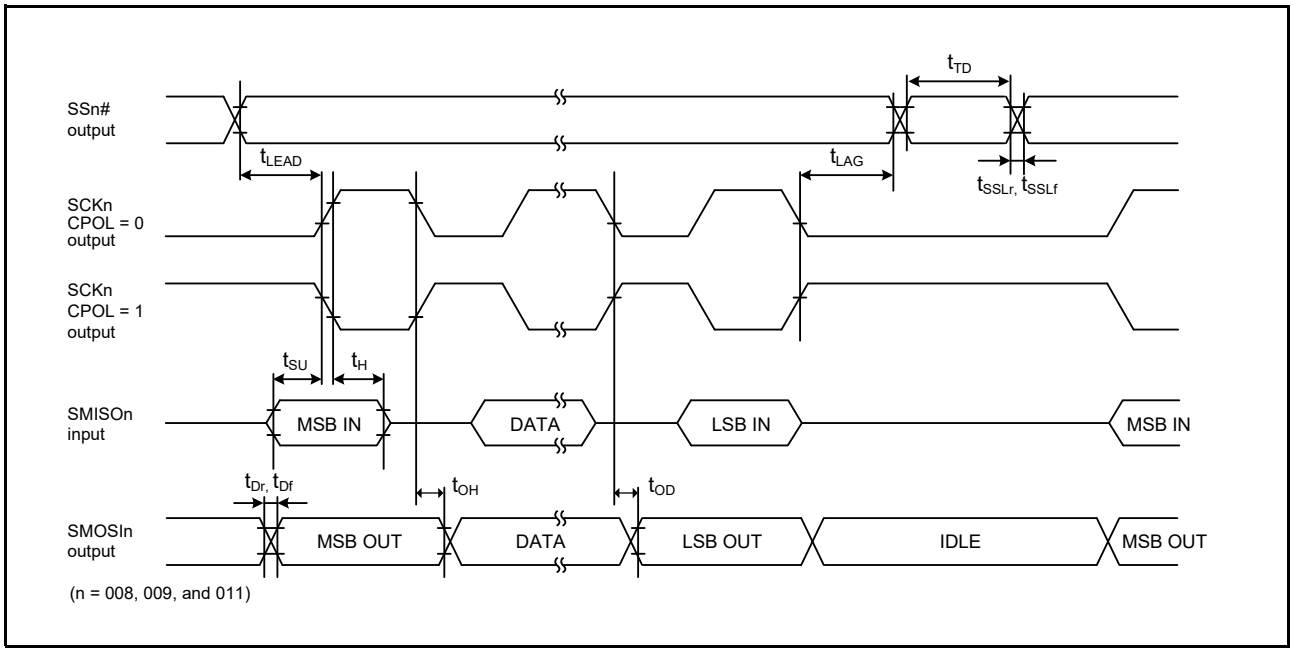


Figure 2.48 Simple SPI Timing (Master, CPHA = 0)

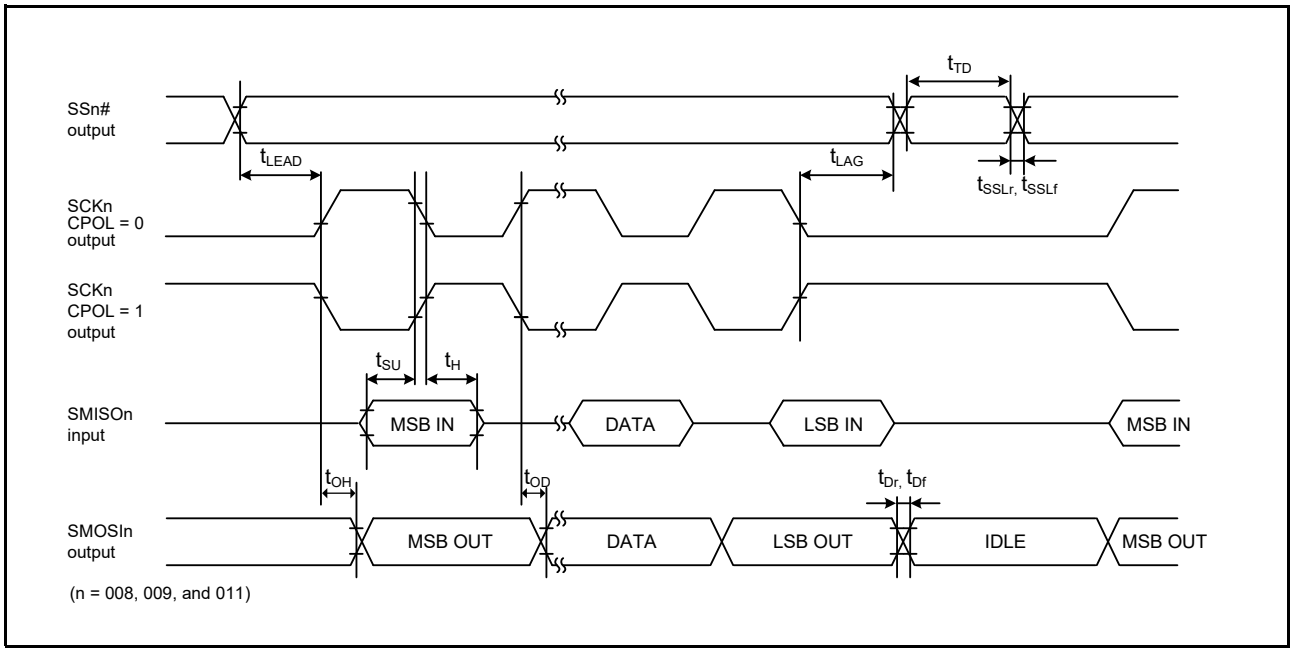


Figure 2.49 Simple SPI Timing (Master, CPHA = 1)

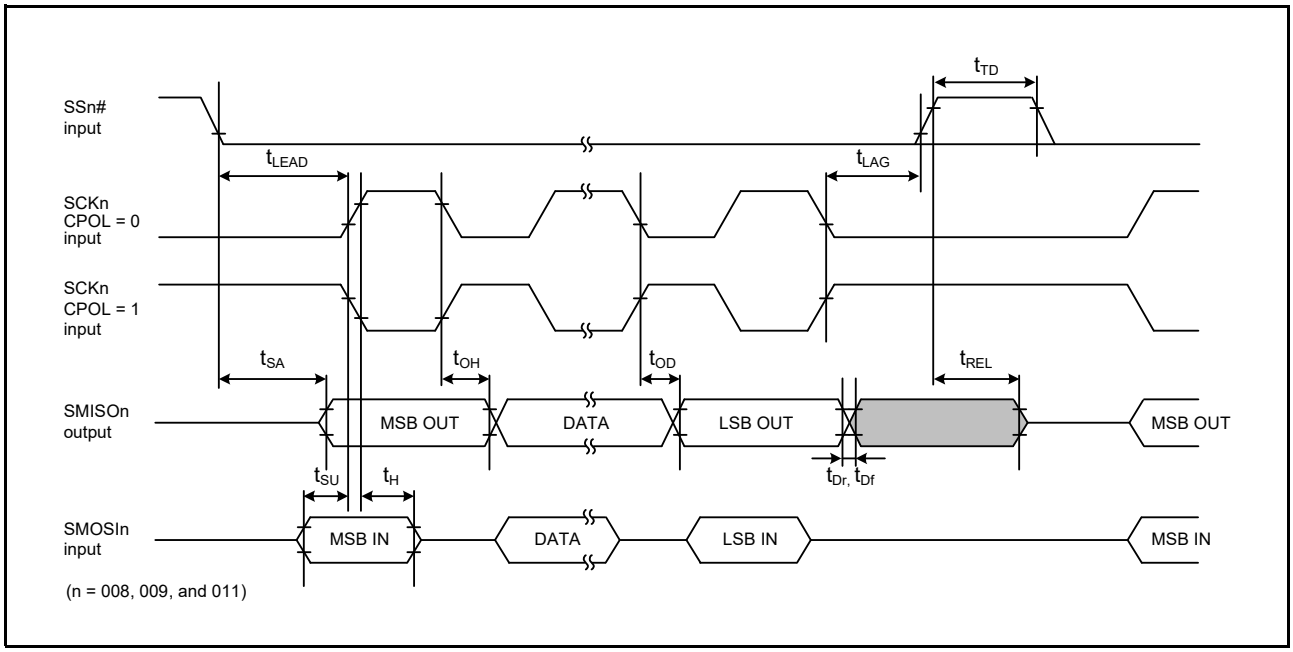


Figure 2.50 Simple SPI Timing (Slave, CPHA = 0)

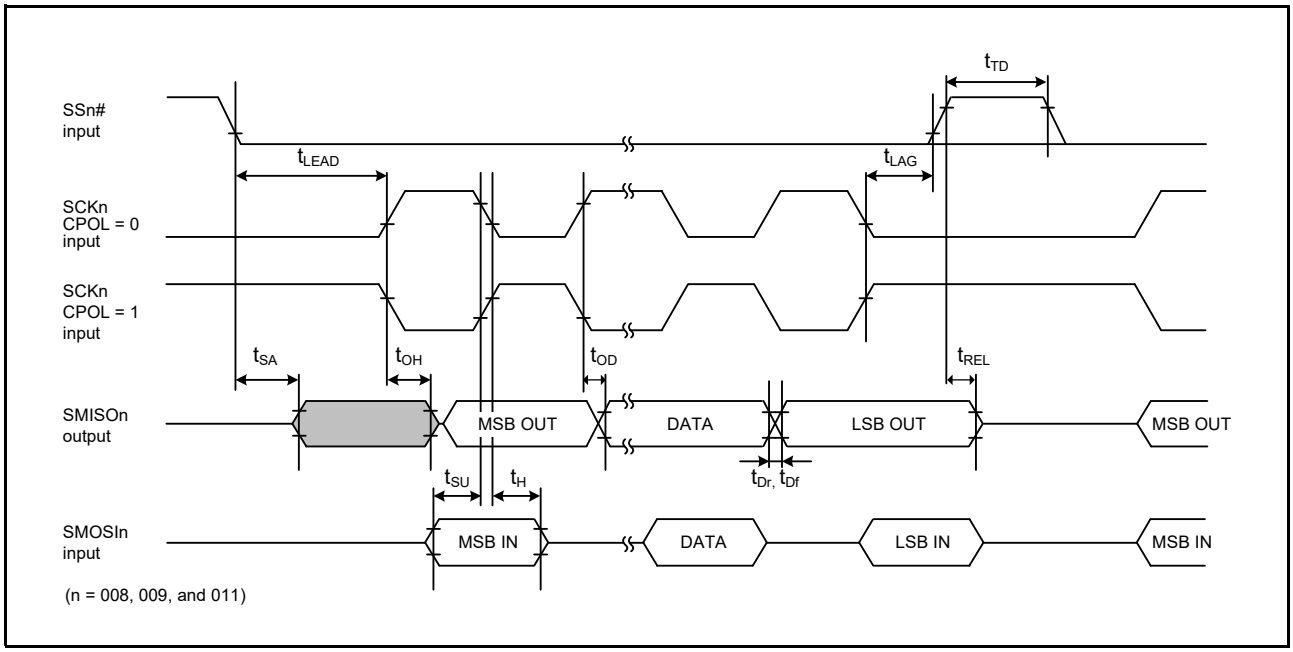


Figure 2.51 Simple SPI Timing (Slave, CPHA = 1)

2.4.5.11 RSPI

Table 2.37 RSPI Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions	
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.52	
		Slave			4	—			
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave			0.4	0.6	t_{SPcyc}		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave			0.4	0.6	t_{SPcyc}		
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns		
		Input			—	1	μs		
	Data input setup time	Master		t_{SU}	6	—	ns	VCC ≥ 4.5 V	Figure 2.53 to Figure 2.58
					11	—		VCC < 4.5 V	
		Slave			8.3	—		Figure 2.53 to Figure 2.58	
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns		
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—			
		Slave			8.3	—			
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}		
		Slave			4	—	t_{PAcyc}		
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}		
		Slave			4	—	t_{PAcyc}		
	Data output delay time	Master		t_{OD}	—	6.3	ns	VCC ≥ 4.5 V	Figure 2.53 to Figure 2.58
					—	11.3		VCC < 4.5 V	
		Slave			—	28		VCC ≥ 4.5 V	
					—	33		VCC < 4.5 V	
	Data output hold time	Master		t_{OH}	0	—	ns	Figure 2.53 to Figure 2.58	
		Slave			0	—			
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns		
		Slave			$4 \times t_{PAcyc}$	—			
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns		
		Input			—	1	μs		
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns		
		Input			—	1	μs		
	Slave access time			t_{SA}	—	28	ns	VCC ≥ 4.5 V	Figure 2.57, Figure 2.58
					—	33		VCC < 4.5 V	
	Slave output release time			t_{REL}	—	28	ns	VCC ≥ 4.5 V	
					—	33		VCC < 4.5 V	

Note 1. t_{PAcyc}: PCLKA cycle

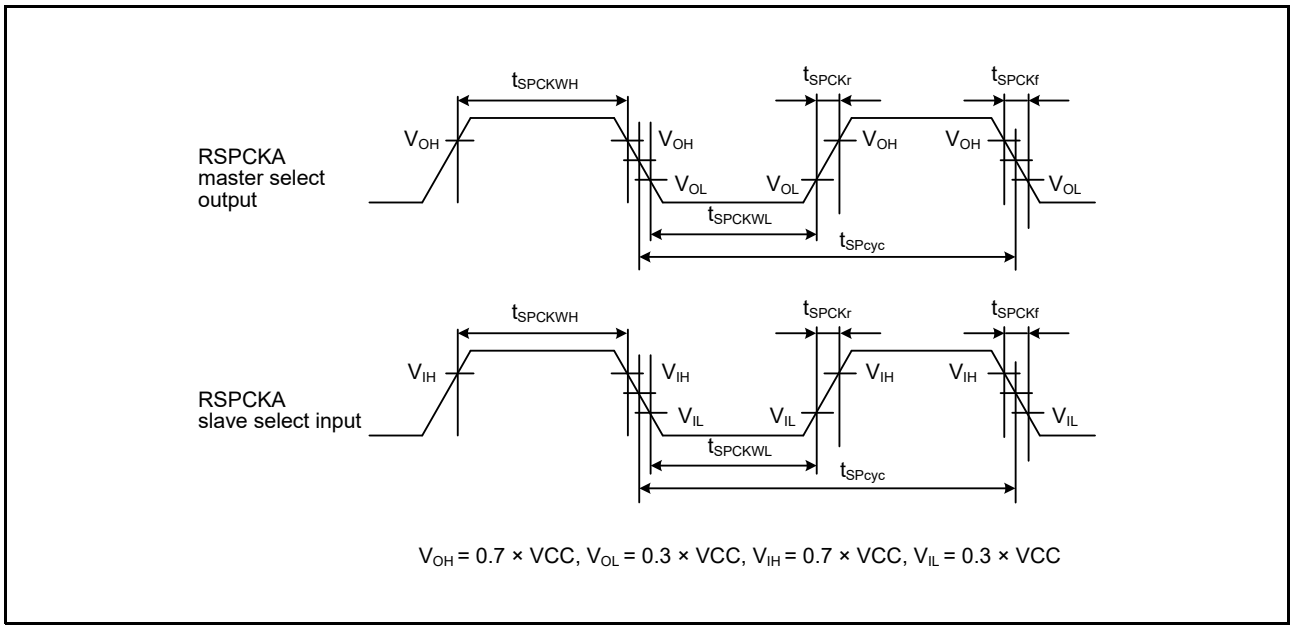


Figure 2.52 RSPI Clock Timing

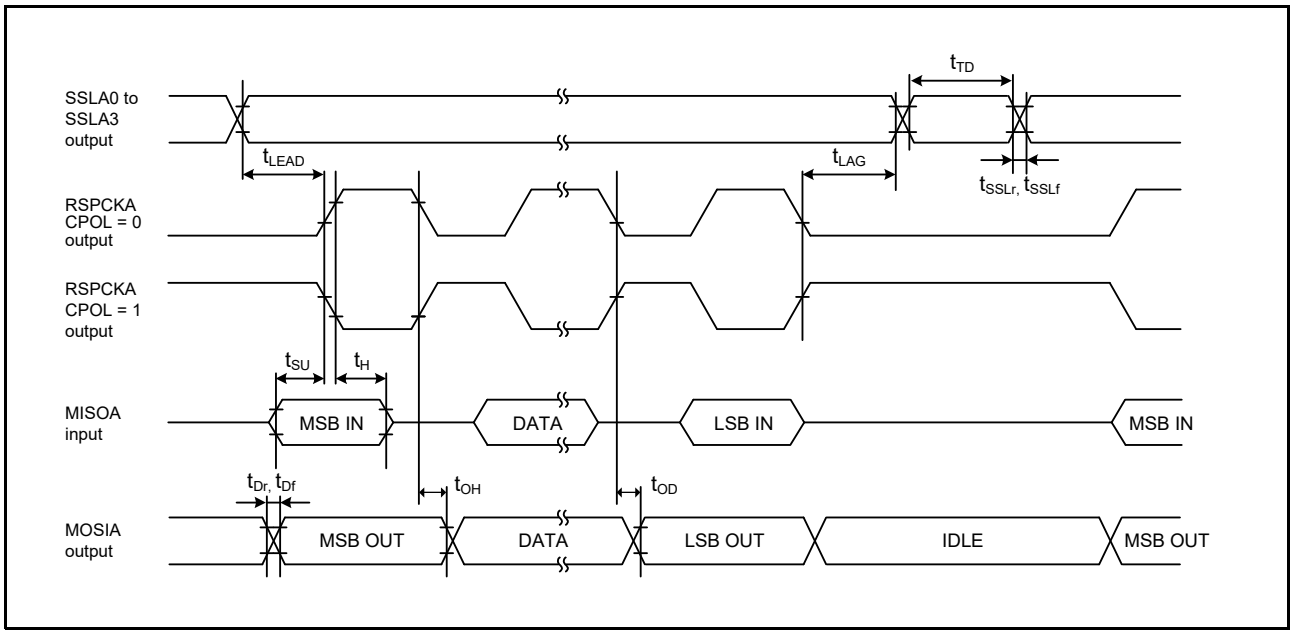


Figure 2.53 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

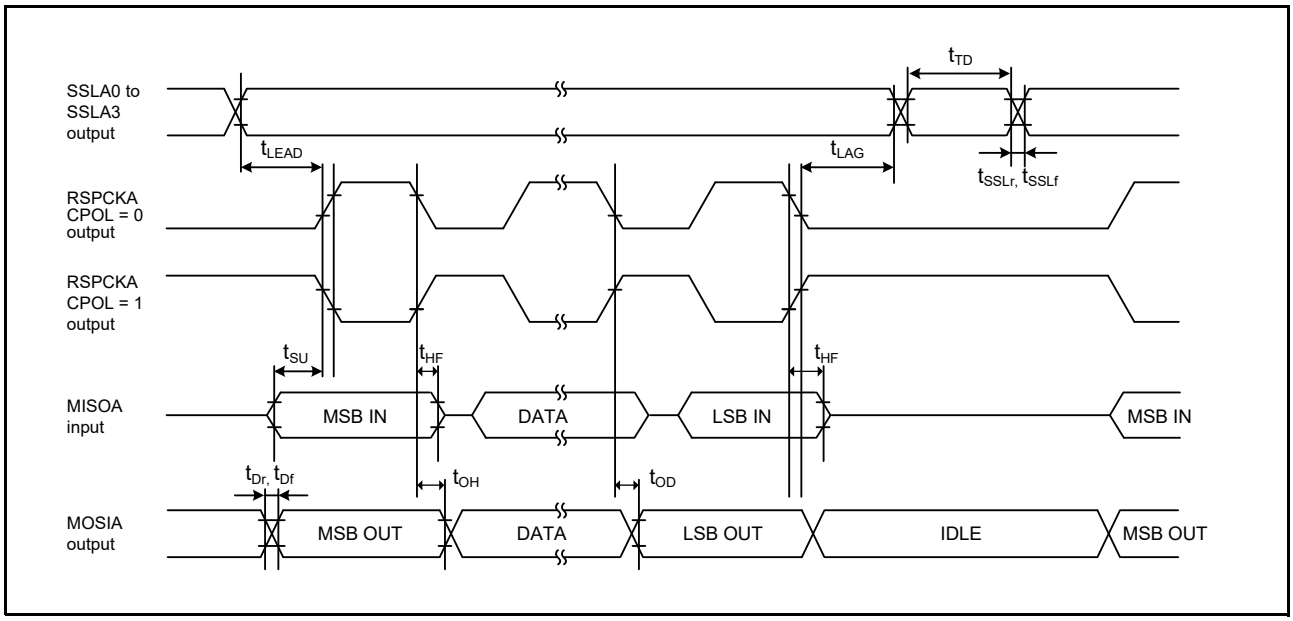


Figure 2.54 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

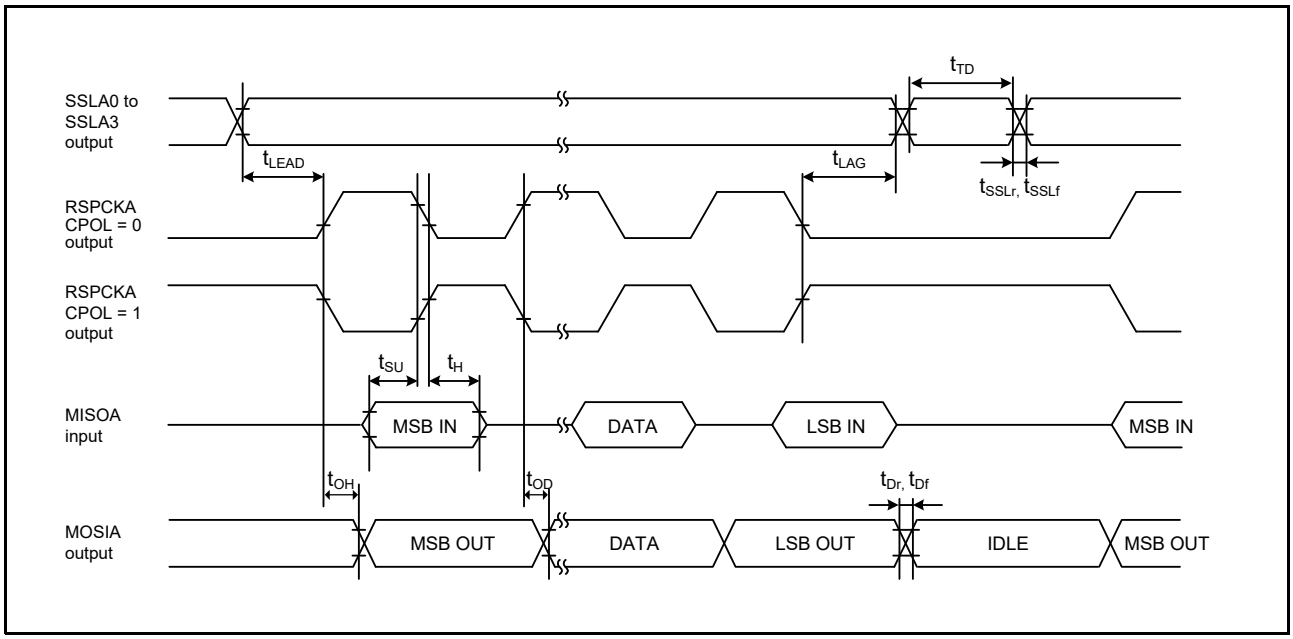


Figure 2.55 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

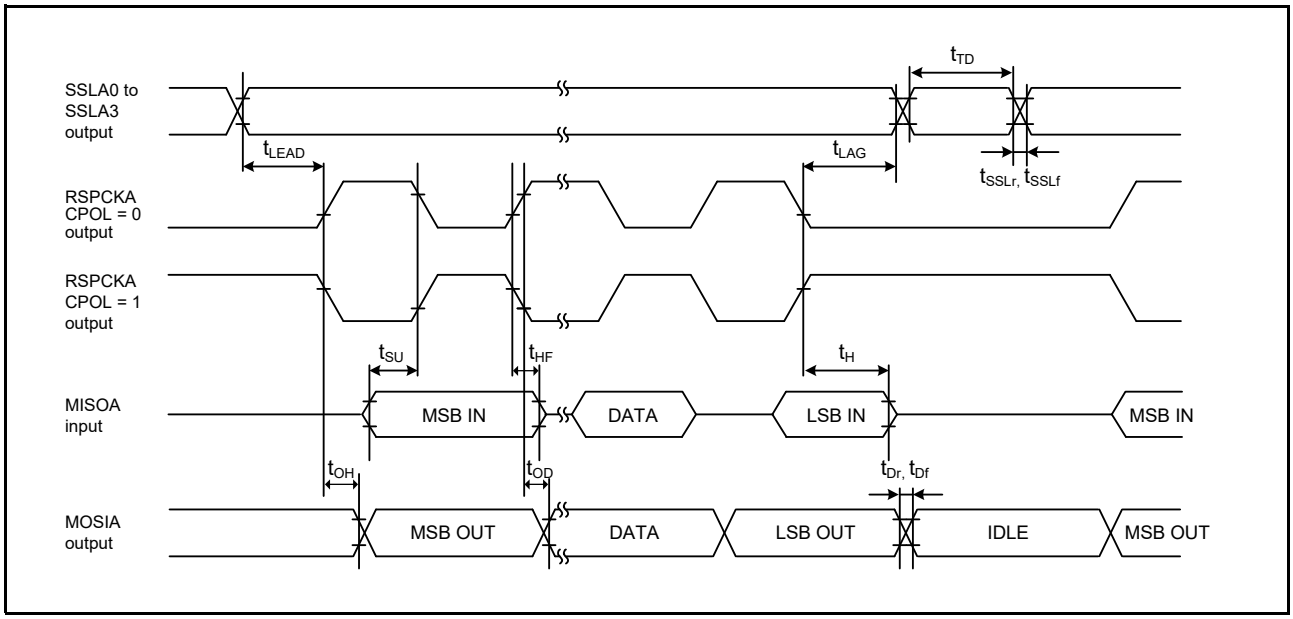


Figure 2.56 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

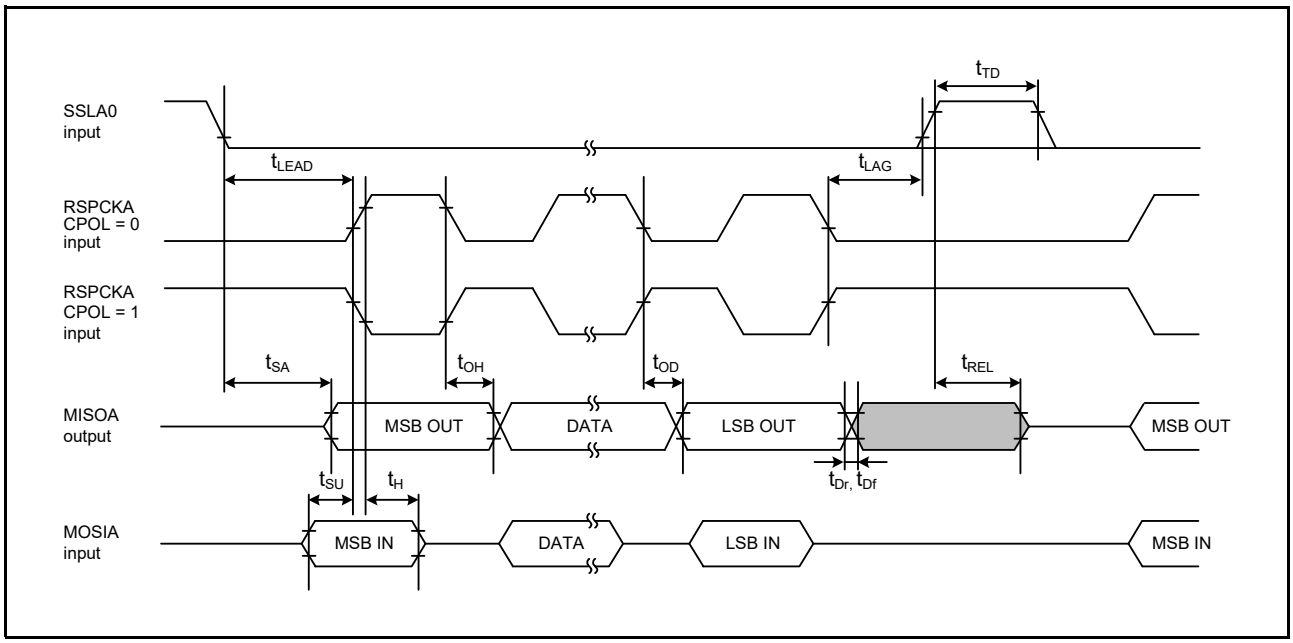


Figure 2.57 RSPI Timing (Slave, CPHA = 0)

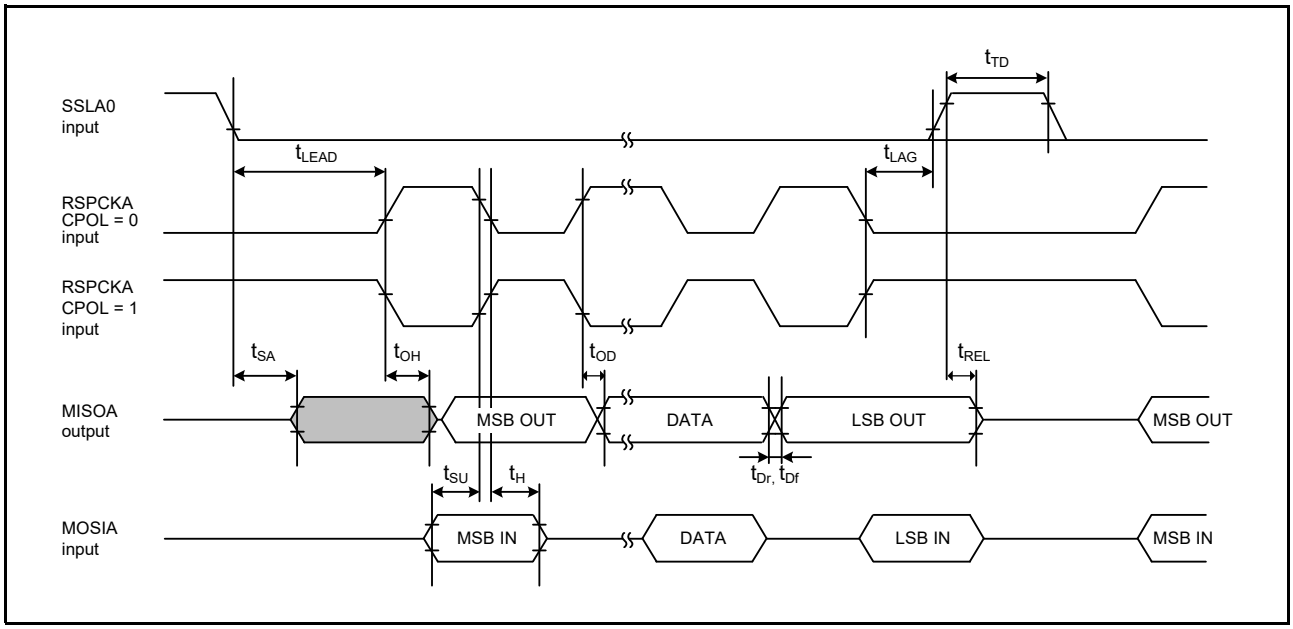


Figure 2.58 RSPI Timing (Slave, CPHA = 1)

2.4.5.12 RSPIA

Table 2.38 RSPIA Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 15 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.59	
		Slave		2	—			
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave		0.4	0.6	t_{SPcyc}		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns		
		Slave		0.4	0.6	t_{SPcyc}		
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns		
		Input		—	1	µs		
	Data input setup time	Master	t_{SU}	0	—	ns	VCC ≥ 4.5 V	Figure 2.60 to Figure 2.66
				2.5	—		VCC < 4.5 V	
		Slave		2.5	—			
	Data input hold time	Master	t_H	7	—	ns		
		Slave		2.5	—			
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}		
		Slave		6	—	t_{PAcyc}		
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}		
		Slave		6	—	t_{PAcyc}		
	Data output delay time	Master	t_{OD}	—	4.5	ns	VCC ≥ 4.5 V	
				—	5.5		VCC < 4.5 V	
		Slave		—	14		VCC ≥ 4.5 V	
				—	18		VCC < 4.5 V	
	Data output hold time	Master	t_{OH}	0	—	ns		
		Slave		0	—			
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns		
		Slave		t_{SPcyc}	—			
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns		
		Input		—	1	µs		
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns		
		Input		—	1	µs		
	Slave access time		t_{SA}	—	20	ns	Figure 2.63, Figure 2.64	
	Slave output release time		t_{REL}	—	20	ns		
	TI SSP SS input setup time	Slave	t_{TISS}	4.5	—	ns	Figure 2.65, Figure 2.66	
	TI SSP SS input hold time	Slave	t_{TISH}	2.5	—	ns		
	TI SSP next-access delay time	Slave	t_{TIND}	$2 \times t_{PAcyc} +$ SLNDL × t_{PAcyc}	—	ns		
	TI SSP SS output delay time	Master	t_{TISSOD}	—	7	ns	Figure 2.62	

Note 1. t_{PAcyc}: PCLKA cycle

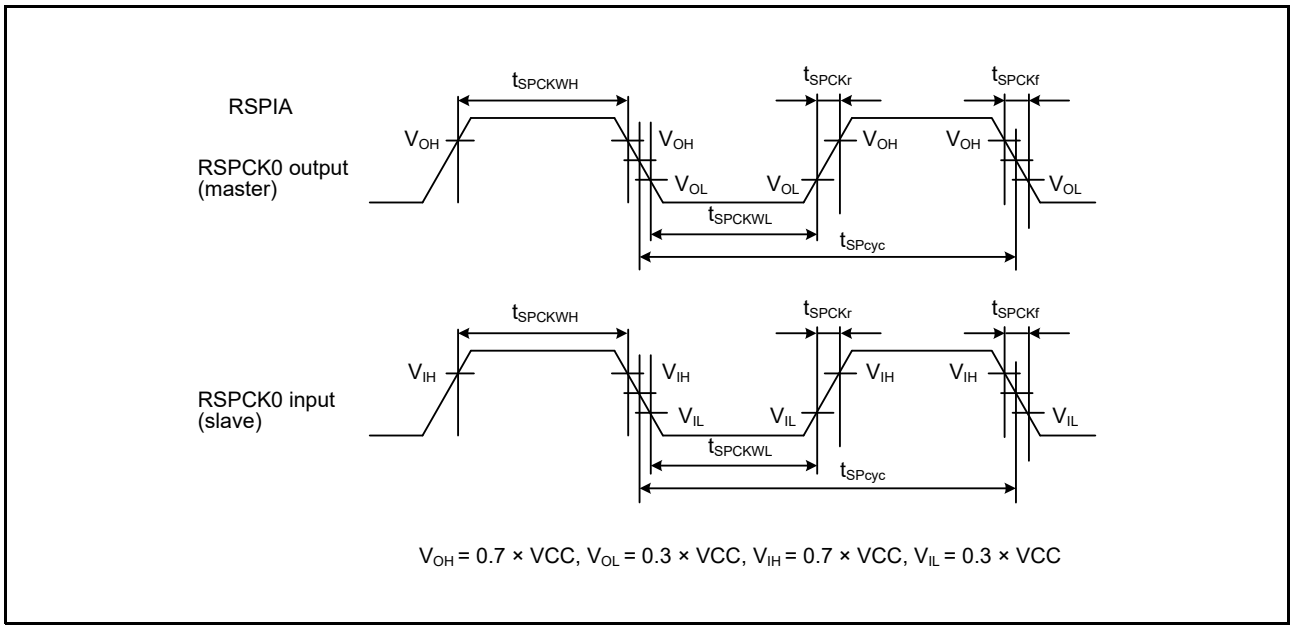


Figure 2.59 RSPIA Clock Timing

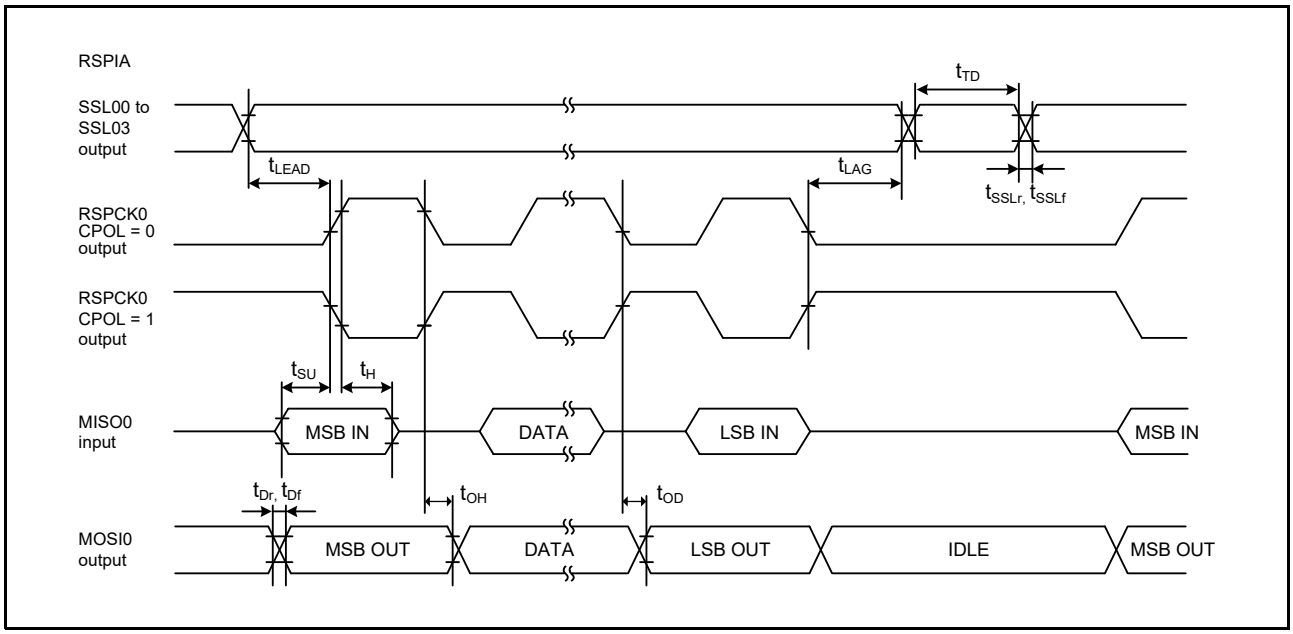


Figure 2.60 RSPIA Timing (Master, Motorola SPI, CPHA = 0)

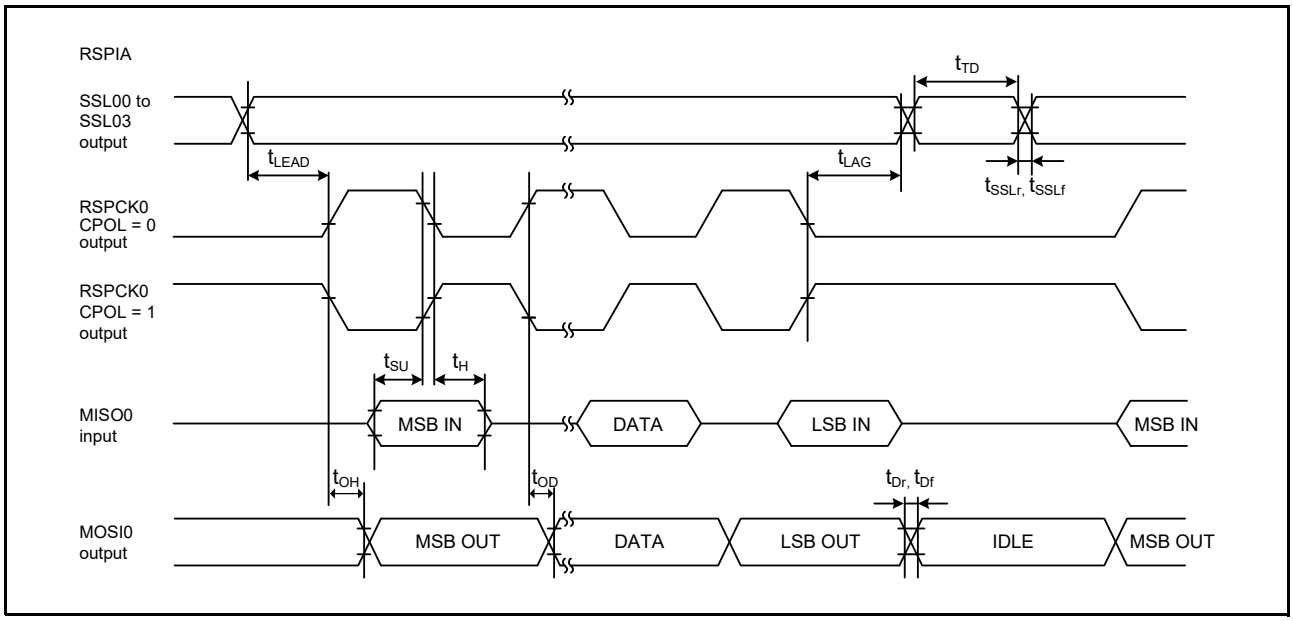


Figure 2.61 RSPIA Timing (Master, Motorola SPI, CPHA = 1)

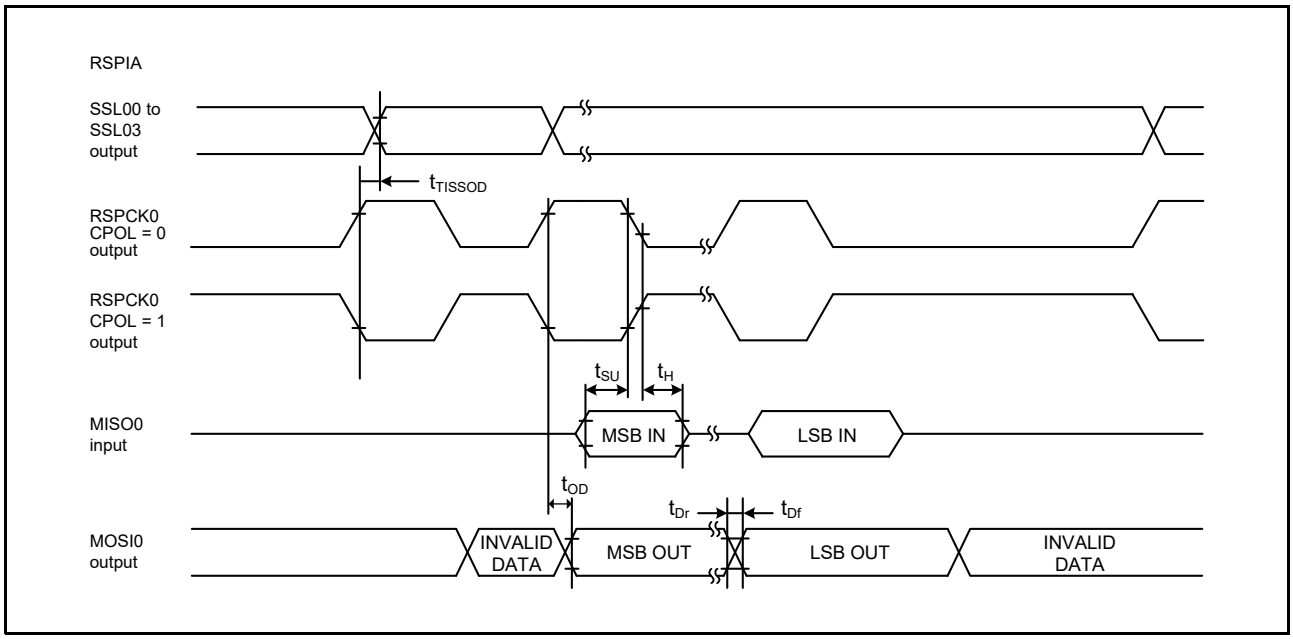


Figure 2.62 RSPIA Timing (Master, TI SSP)

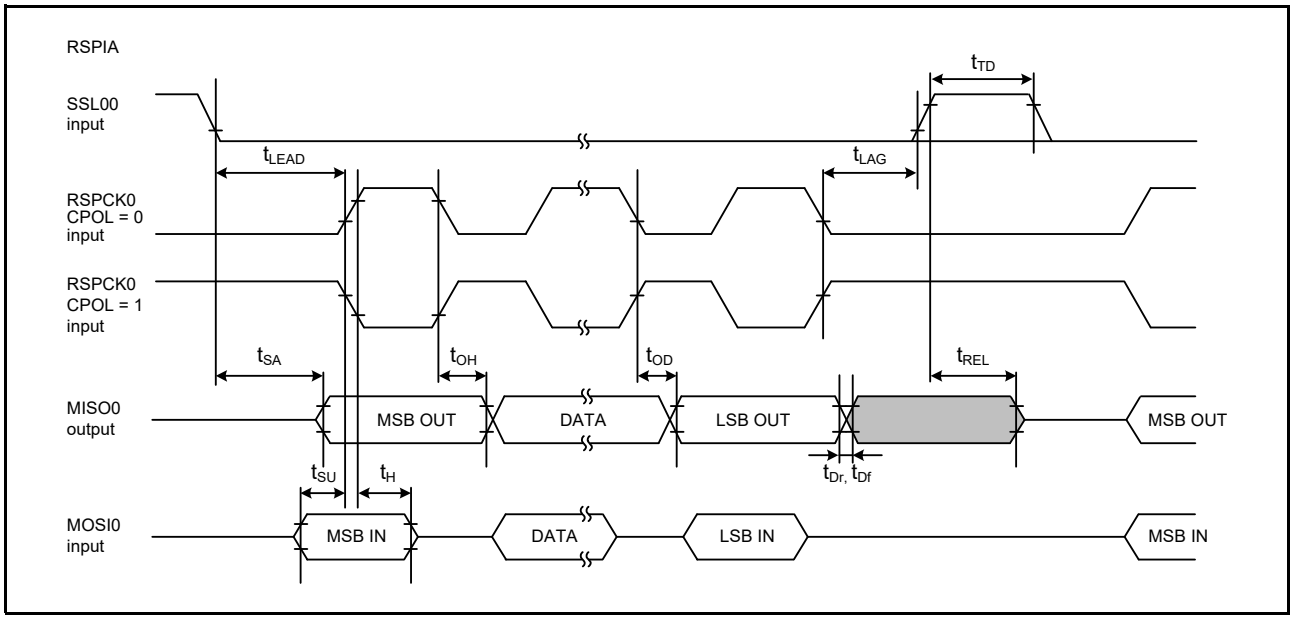


Figure 2.63 RSPIA Timing (Slave, Motorola SPI, CPHA = 0)

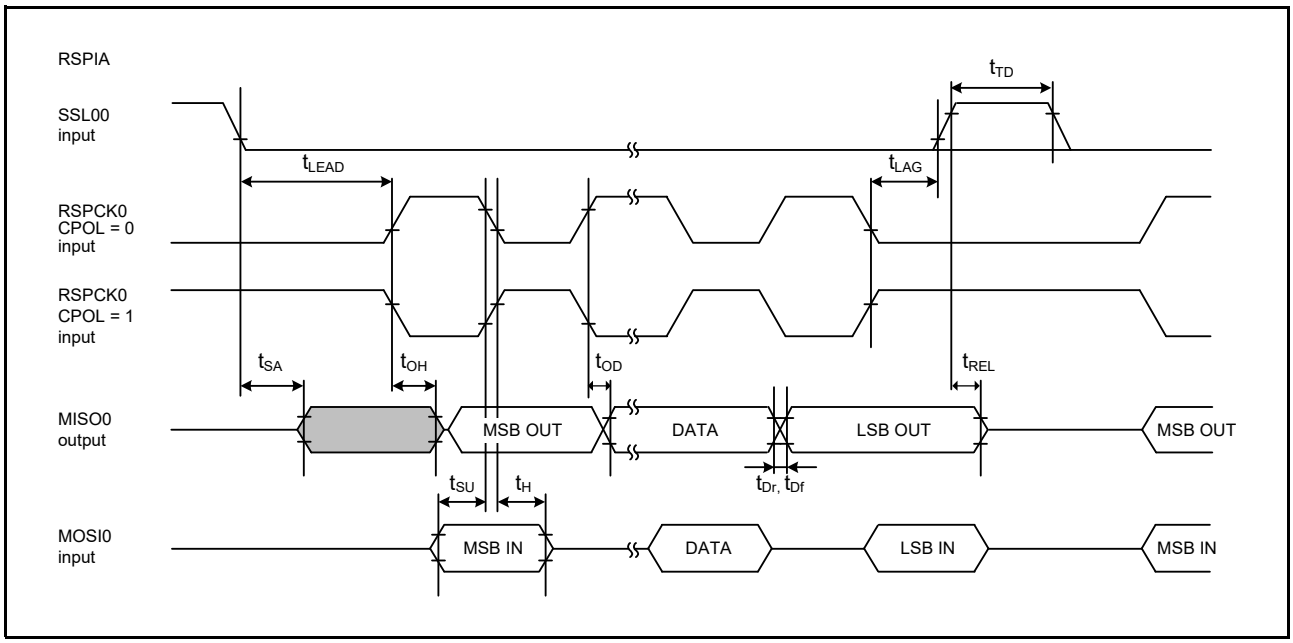


Figure 2.64 RSPIA Timing (Slave, Motorola SPI, CPHA = 1)

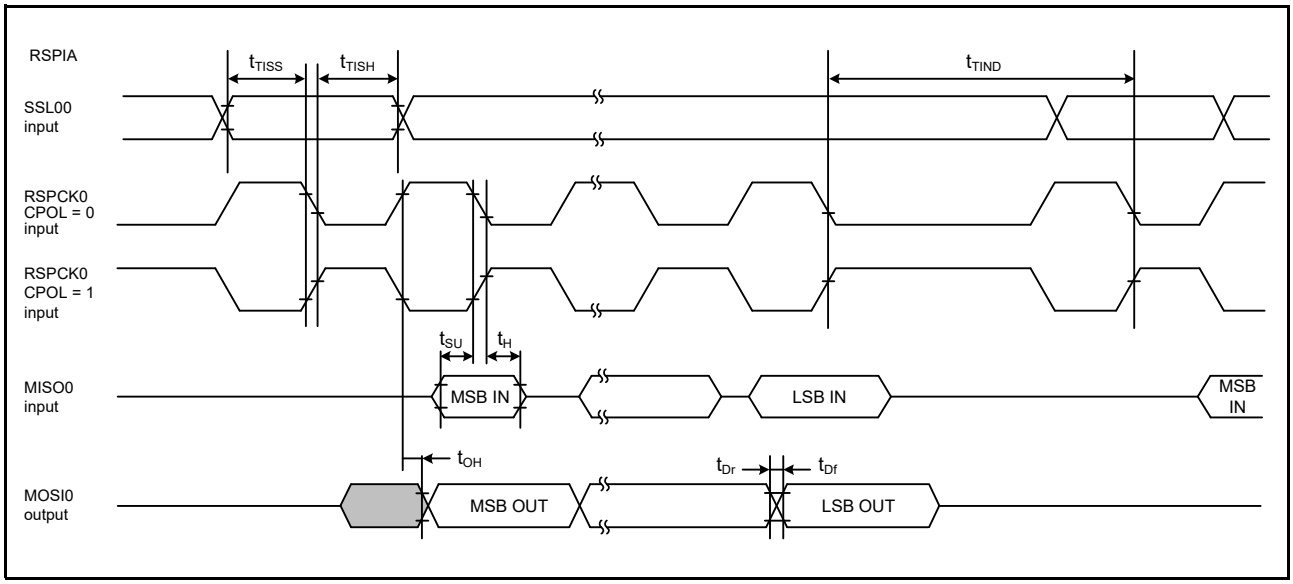


Figure 2.65 RSPIA Timing (Slave, TI SSP, Transmit with Delay between Frames)

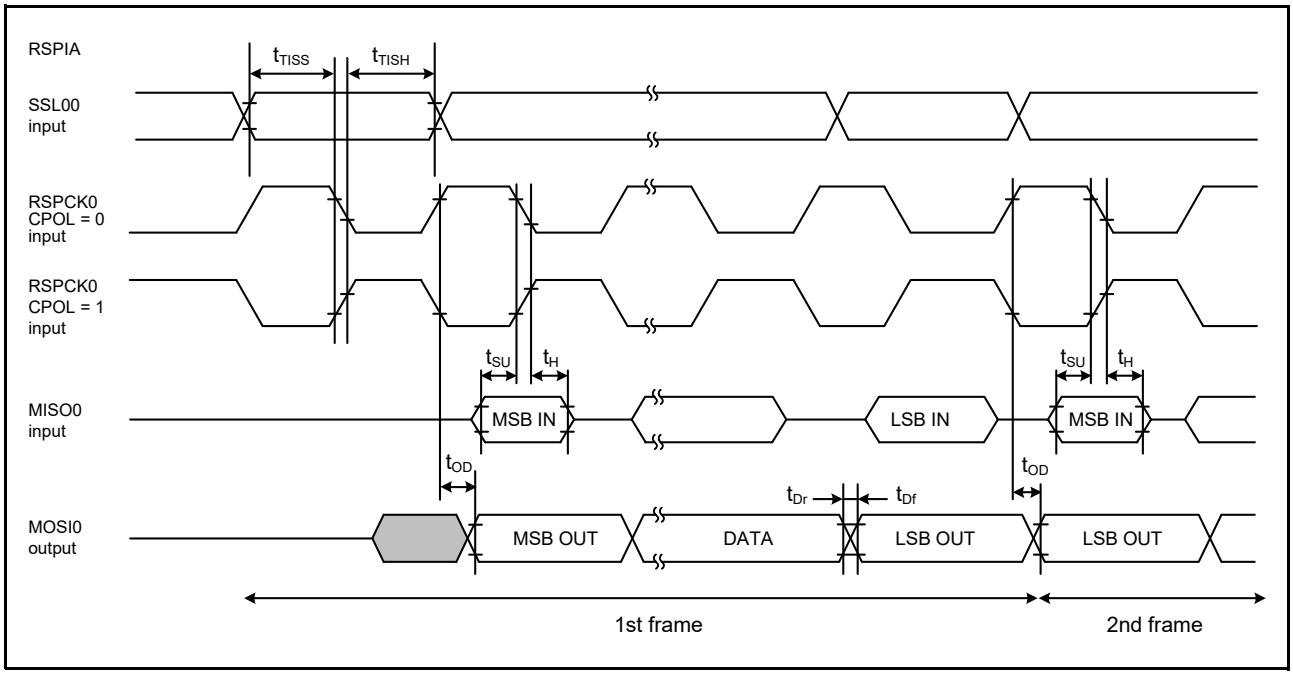


Figure 2.66 RSPIA Timing (Slave, TI SSP, Transmit with No Delay between Frames)

2.4.5.13 RIIC

Table 2.39 RIIC Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.*1	Unit	Test Conditions*3
RIIC (Standard-mode, SMBus)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.67
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—		
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—		
	SCL, SDA input rise time	t_{Sr}	—	1000		
	SCL, SDA input fall time	t_{Sf}	—	300		
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}		
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—		
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—		
	Restart condition input setup time	t_{STAS}	1000	—		
	Stop condition input setup time	t_{STOS}	1000	—		
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—		
	Data input hold time	t_{SDAH}	0	—		
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—		
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—		
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5 V)	300		
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5 V)	300		
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}		
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—		
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—		
	Restart condition input setup time	t_{STAS}	300	—		
	Stop condition input setup time	t_{STOS}	300	—		
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—		
	Data input hold time	t_{SDAH}	0	—		
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. C_b is the total capacitance of the bus lines.
Note 3. When VCC ≥ 4.5 V, VOLSR.RICVLS = 0
When VCC < 4.5 V, VOLSR.RICVLS = 1

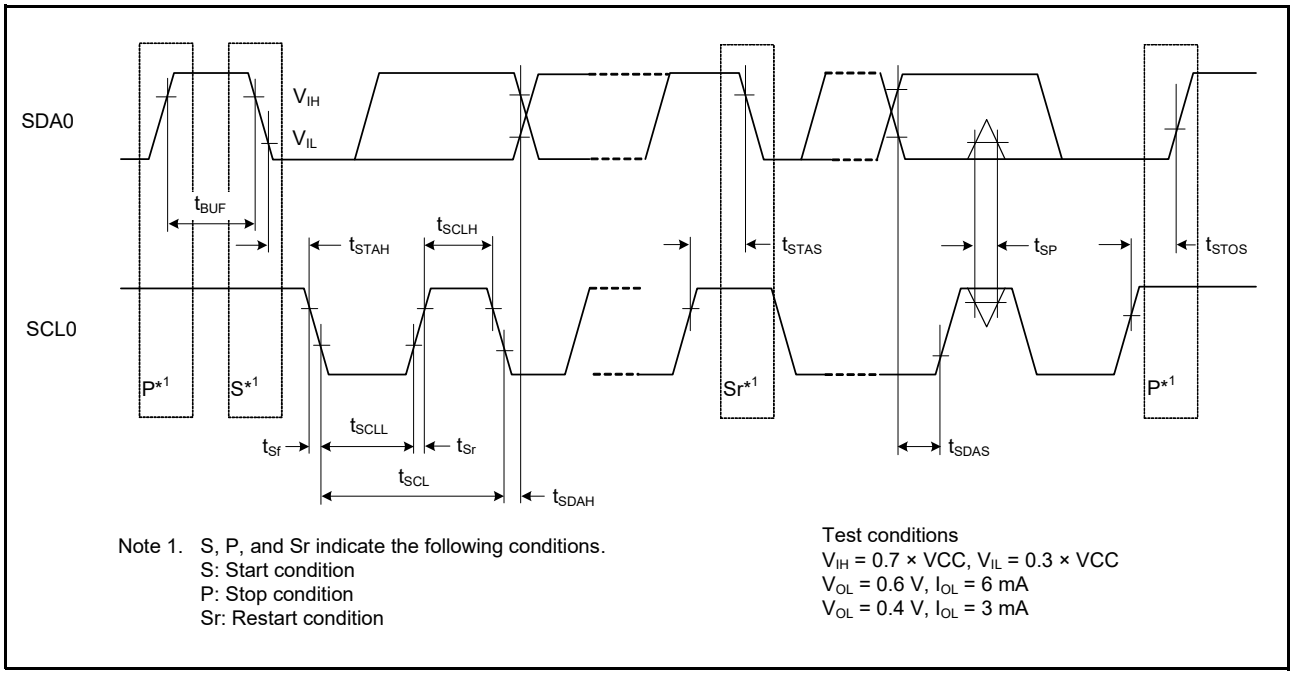


Figure 2.67 RIIC Bus Interface Input/Output Timing

2.4.5.14 RI3C

Table 2.40 RI3C Timing (Open Drain Timing Parameters)

Conditions: VCC = AVCC0 = AVCC1 = AVCC2 = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
SCL clock low period	t_{LOW_OD}	200*1, *2	—	—	ns	Figure 2.68
	$t_{DIG\_OD\_L}$	t_{LOW_ODmin} + t_{fDA_ODmin}	—	—		
SDA signal fall time	t_{fDA_OD}	t_{CF}	—	33	ns	Figure 2.68
SDA data setup time open drain mode	t_{SU_OD}	3*1	—	—	ns	Figure 2.68, Figure 2.69
Clock after START (S) condition	t_{CAS}	38.4 ns*3	—	For ENTAS0: 1 µs	—	Figure 2.68
			—	For ENTAS1: 100 µs		
			—	For ENTAS2: 2 ms		
			—	For ENTAS3: 50 ms*4		
Clock before STOP (P) condition	t_{CBP}	$t_{CASmin}/2$	—	—	sec	Figure 2.70
Current controller to secondary controller overlap time during handoff	$t_{CRHPOverlap}$	$t_{DIG\_OD\_Lmin}$	—	—	ns	Figure 2.71
Bus available condition	t_{AVAL}	1*5	—	—	µs	
Bus idle condition	t_{IDLE}	1	—	—	ms	
Time internal where new controller not driving SDA low	$t_{NEWCRLock}$	$t_{AVALmin}$	—	—	µs	Figure 2.71

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_ODmin}$.
Note 2. The controller may use a shorter low period if it knows that this is safe, i.e., that SDA is already above V_{IH}.
Note 3. On a legacy bus where I²C devices need to see start, the t_{CAS} Min value is further constrained.
Note 4. Targets that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 5. On a mixed bus with Fm legacy I²C devices, t_{AVAL} is 300 ns shorter than the Fm bus free condition time (t_{BUF})

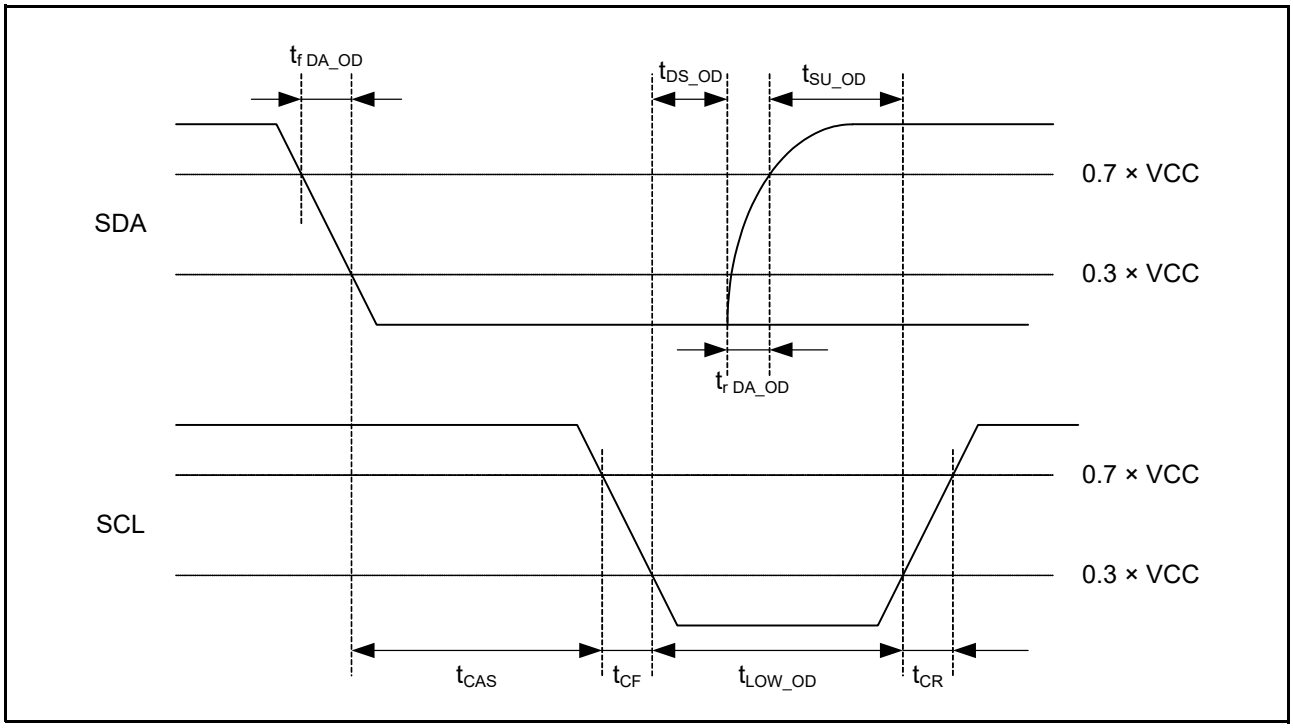


Figure 2.68 RI3C Start Condition Timing

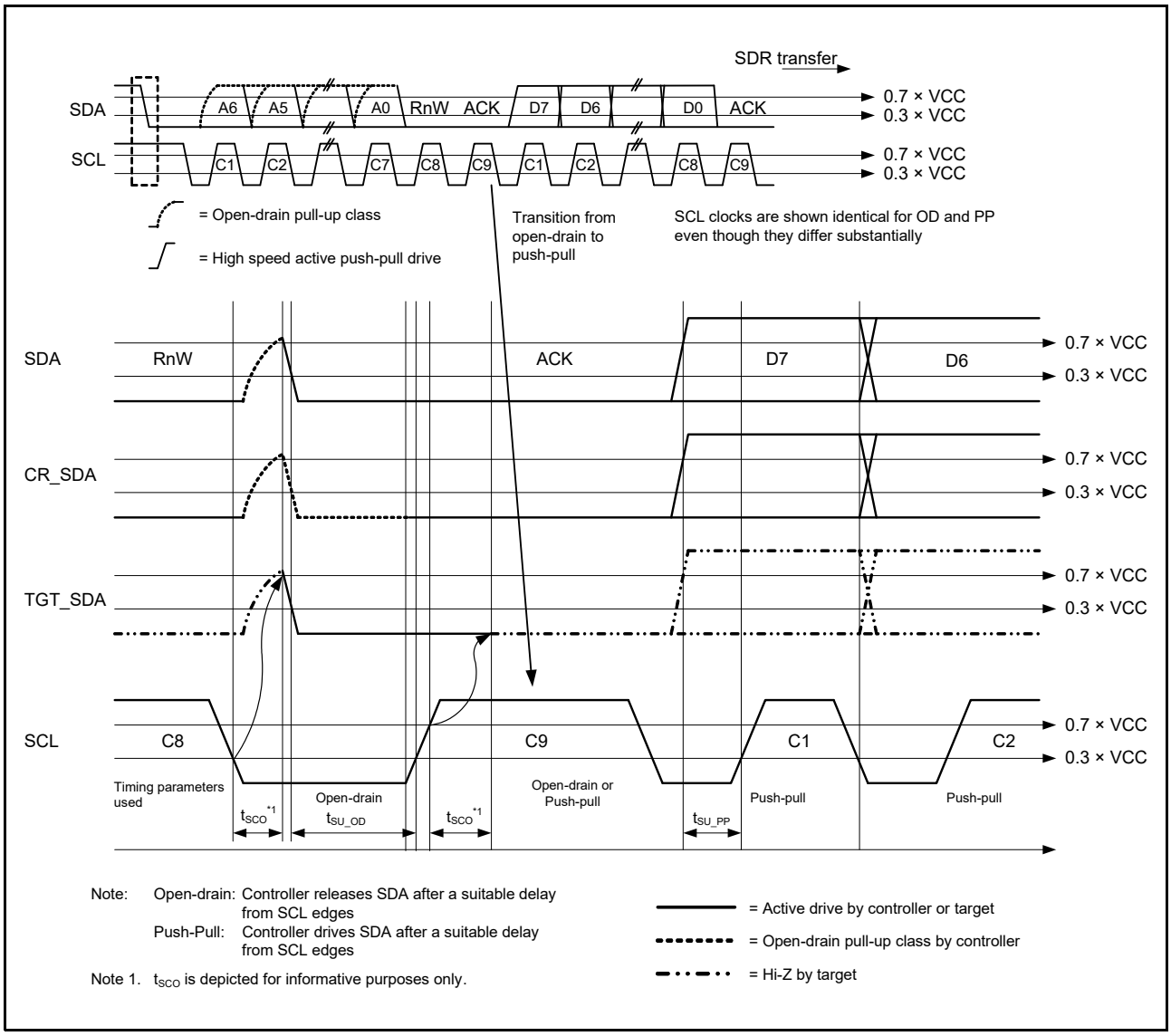


Figure 2.69 RI3C Data Transfer — ACK by Target

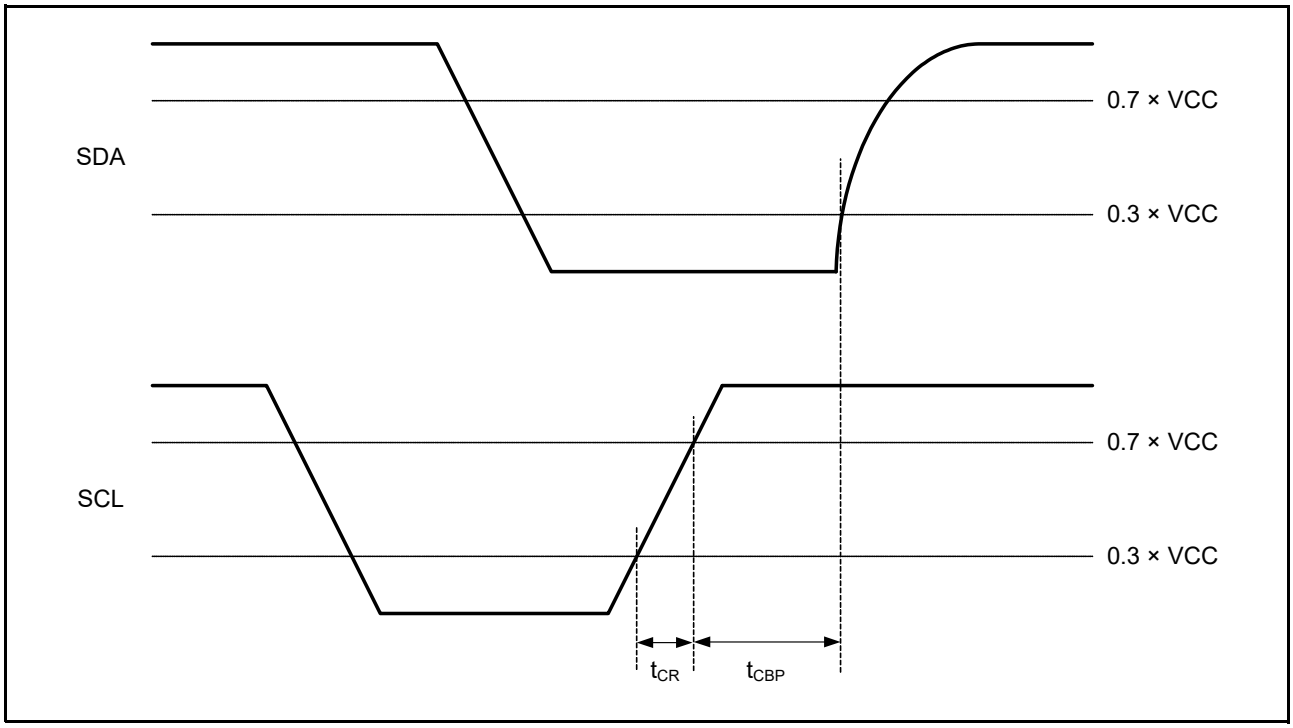


Figure 2.70 RI3C Stop Condition Timing

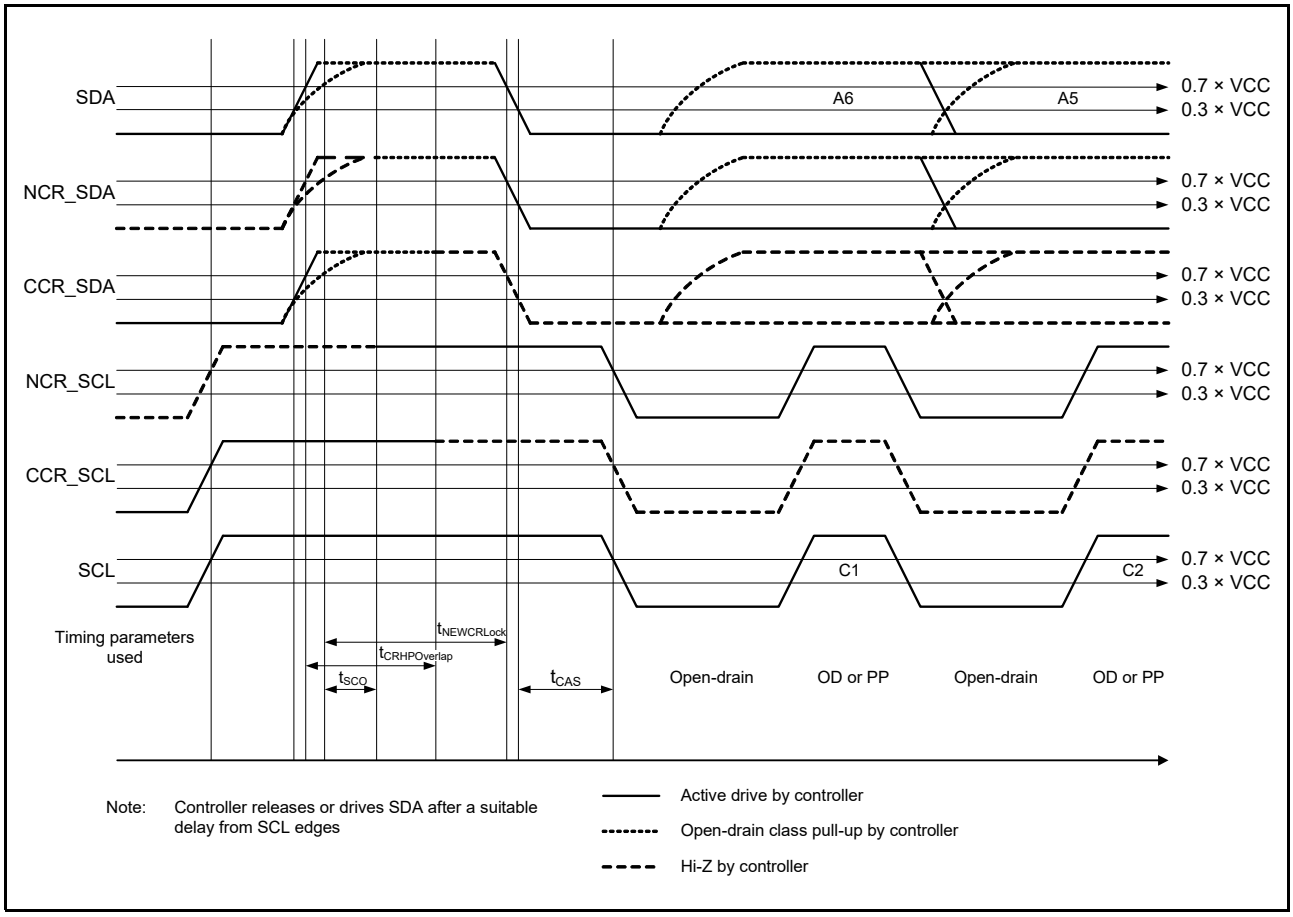


Figure 2.71 RI3C Output Timing

Table 2.41 RI3C Timing (Push-Pull Timing Parameters for SDR)

Conditions: VCC = AVCC0 = AVCC1 = AVCC2 = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
SCL clock frequency		f_{SCL}	0.01*1	—	10	MHz	
SCL clock low period		t_{LOW}	35	—	—	ns	Figure 2.72
		t_{DIG_L}	50*2, *3	—	—	ns	
SCL clock high period		t_{HIGH}	35	—	—	ns	
		t_{DIG_H}	50*2	—	—	ns	
Clock in to data out for target		t_{SCO}	—	—	42	ns	Figure 2.73
SCL clock rise time		t_{CR}	—	—	150 * 1 /f_{SCL} (capped at 60)	ns	Figure 2.72
SCL clock fall time		t_{CF}	—	—	150 * 1 /f_{SCL} (capped at 60)	ns	
SDA signal data hold in push-pull mode	Controller	t_{HD_PP}	t_{CR} + 3*3, t_{CF} + 3*3	—	—	—	Figure 2.74
	Target	t_{HD_PP}	0	—	—	—	Figure 2.75
SDA signal data setup in push-pull mode		t_{SU_PP}	3	—	—	ns	Figure 2.73, Figure 2.74
Clock after repeated start (Sr)		t_{CASr}	t_{CASmin}/2	—	N/A	ns	Figure 2.76
Clock before repeated start (Sr)		t_{CBSr}	t_{CASmin}/2	—	N/A	ns	Figure 2.76
Capacitive load per bus line (SDA/SCL)		C_b*4	—	—	50	pF	

Note 1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
Note 2. t_{DIG_L} and t_{DIG_H} are the clock low and high periods as seen at the receiver end of the I3C bus using V_{IL} and V_{IH}.
Note 3. As both edges are used, the hold time must be satisfied for the respective edges, for example, t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.
Note 4. C_b is the total capacitance of the bus lines.

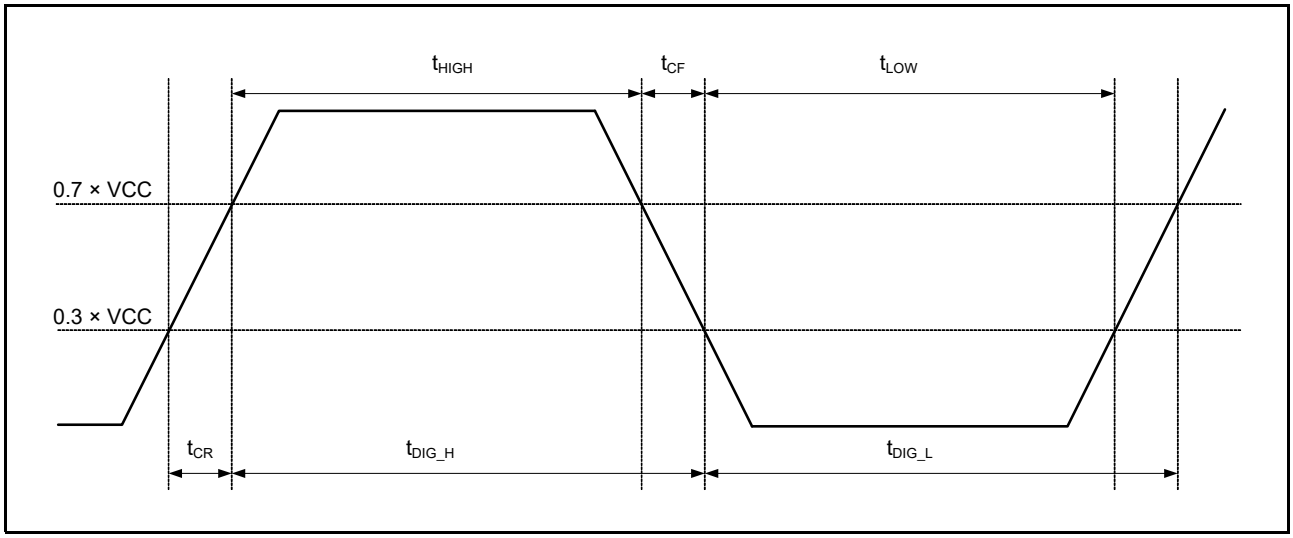


Figure 2.72 t_{DIG_H} and t_{DIG_L}

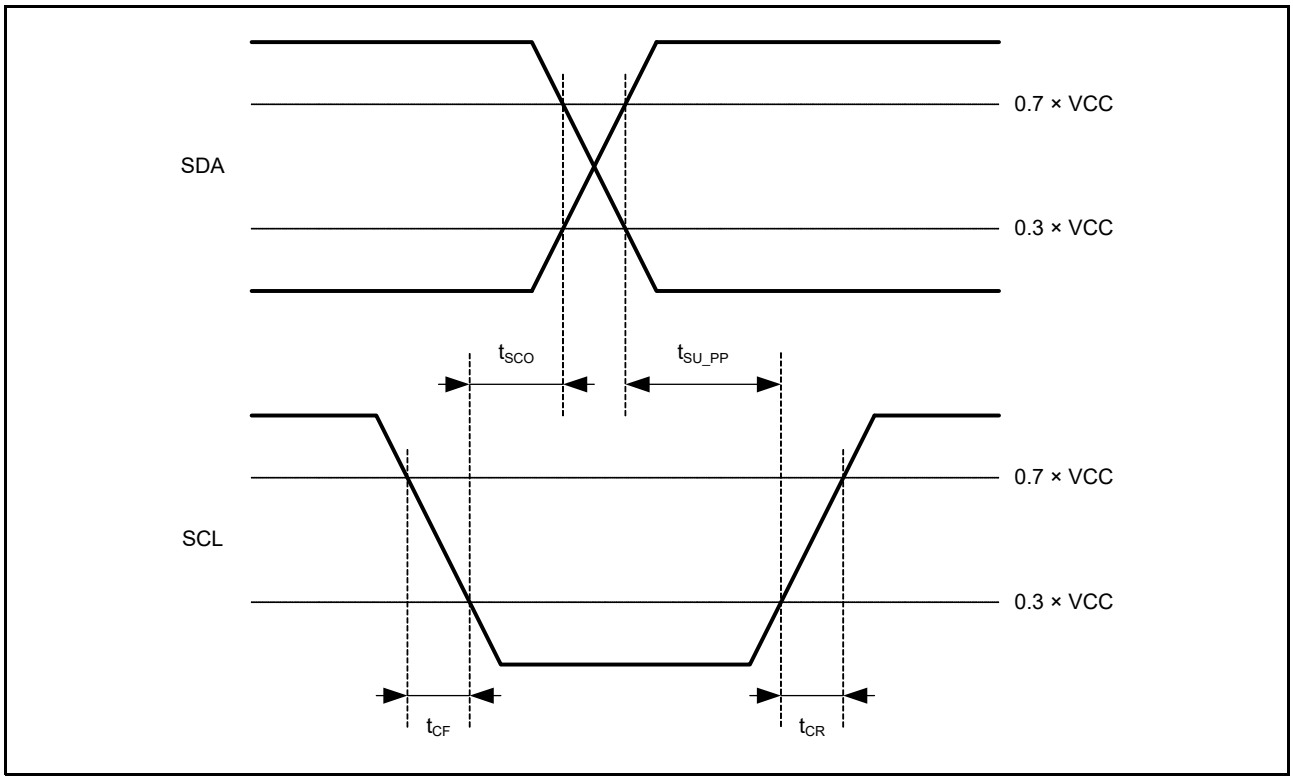


Figure 2.73 RI3C Target Output Timing

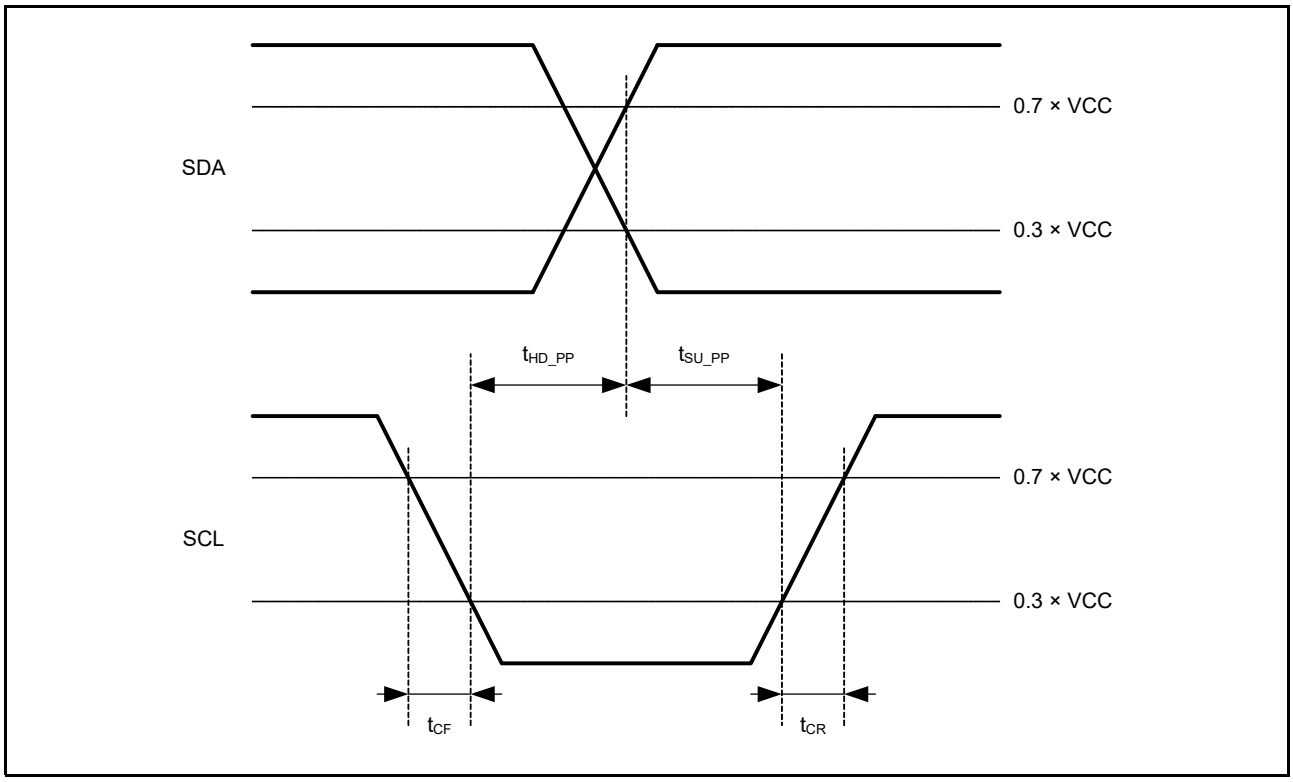


Figure 2.74 RI3C Bus Controller Output Timing

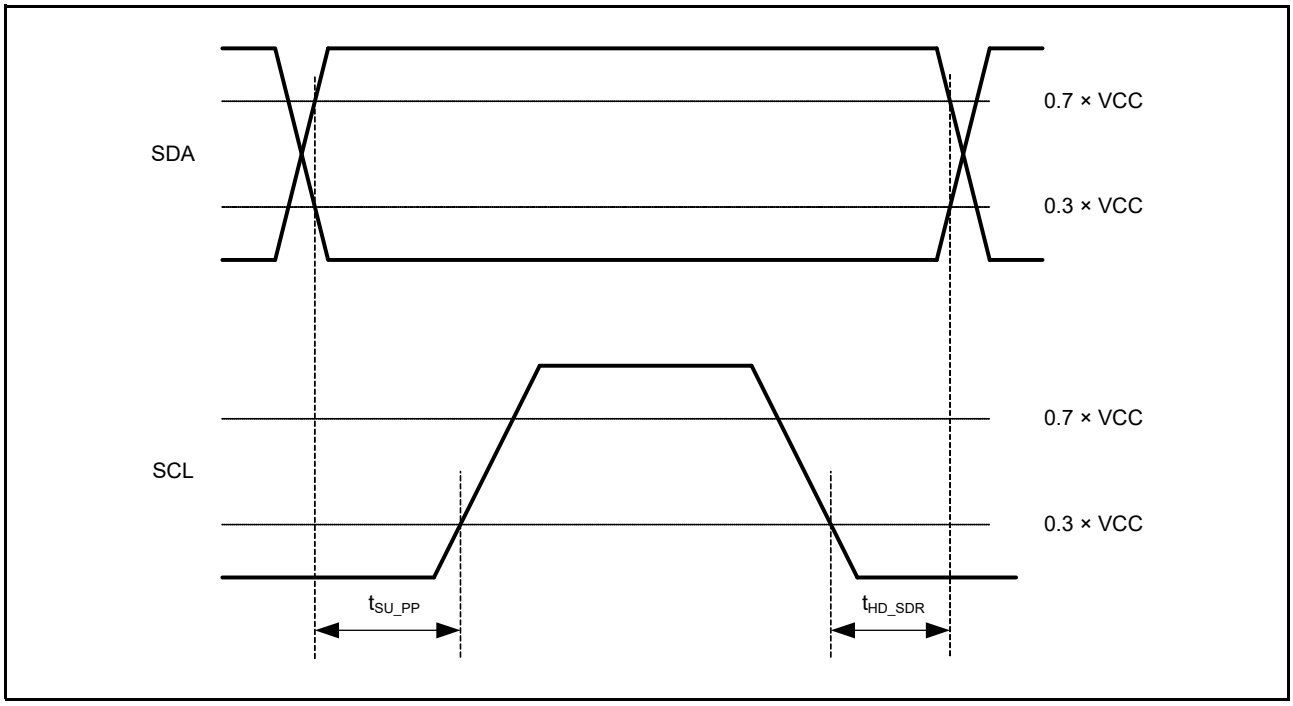


Figure 2.75 Controller SDR Timing

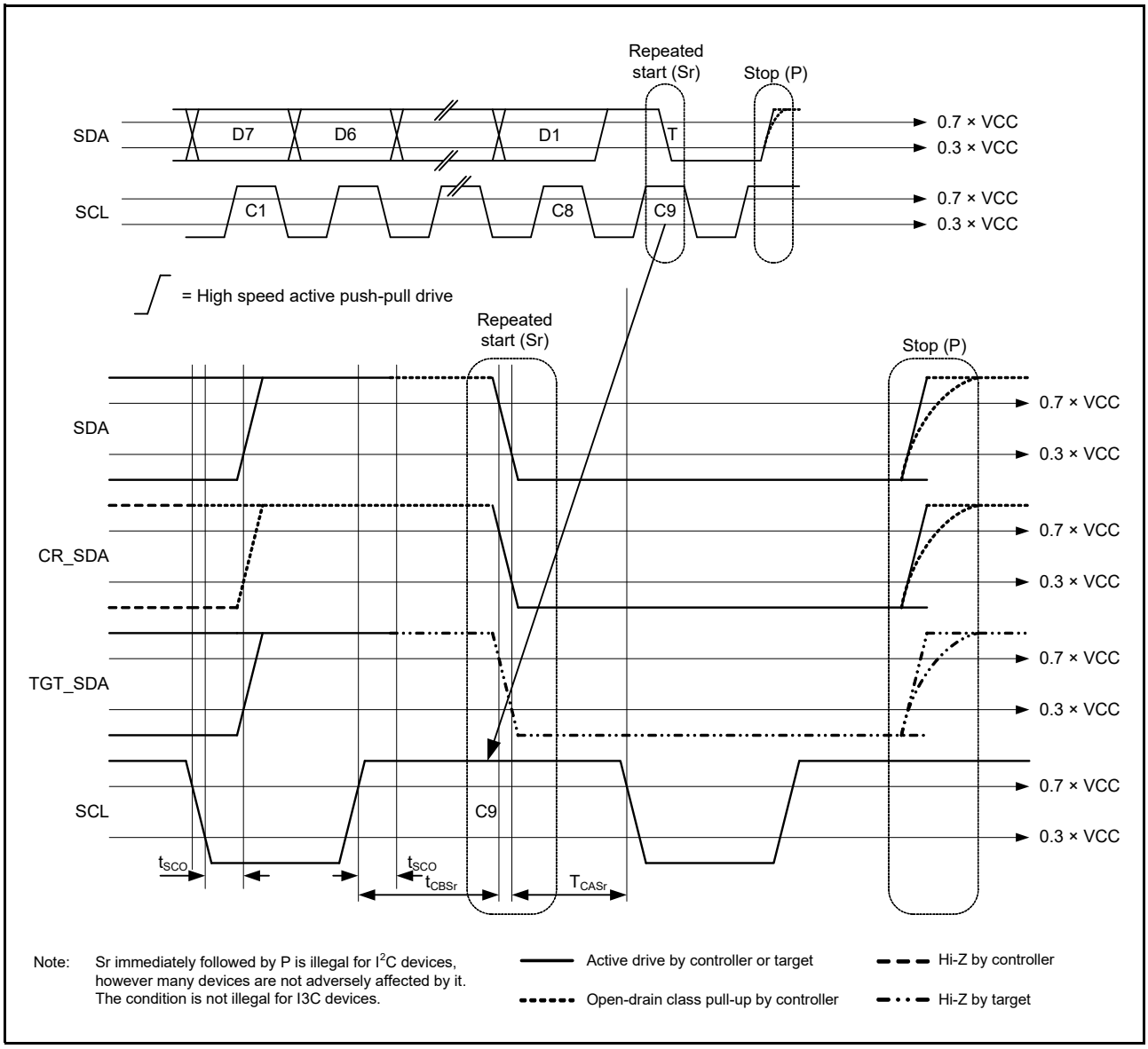


Figure 2.76 T-Bit When Controller Ends Read with Repeated Start and Stop

2.4.5.15 HRPWM

Table 2.42 HRPWM Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz,
Output load conditions: $V_{OH} = 0.5 \times VCC$, $V_{OL} = 0.5 \times VCC$, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Input frequency (f_{IN})	80	—	120	MHz	
Resolution	—	260	—	ps	f_{IN} = 120 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. The value is that difference from code to code normalized by the resolution (1 LSB).

2.4.5.16 CANFD

Table 2.43 CANFD Timing

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Max.	Unit
Classic CAN mode	Bit rate for communications		—	1	Mbps
CAN FD mode	Bit rate for communications		—	1	Mbps
	Bit rate for communications (only for data)		—	5	

2.5 A/D Conversion Characteristics

Table 2.44 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, 4.5 V ≤ AVCC0 = AVCC1 = AVCC2 ≤ 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz*1,
Source impedance = 1.0 kΩ

Item				Min.	Typ.	Max.	Unit	Test Conditions
Resolution				12	12	12	Bit	
Analog input capacitance				—	—	30	pF	
Conversion time*2 (Operation at PCLKD = 60 MHz)	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use	Constant sampling enabled	1.00	—	—	μs	• Sampling time: 24 PCLKD
			Constant sampling disabled	1.40	—	—		• Sampling time of channel-dedicated sample-and-hold circuits: 24 PCLKD • Sampling time: 24 PCLKD
		Channel-dedicated sample-and-hold circuits not in use		0.90	—	—		• Sampling time: 30 PCLKD
	AN003, AN103			0.90	—	—		• Sampling time: 30 PCLKD
	AN200 to AN211			0.95	—	—		• Sampling time: 33 PCLKD
	AN216 to AN217			1.05	—	—		• Sampling time: 39 PCLKD
Offset error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±6.0	LSB	AN000 to AN002, AN100 to AN102 = 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±5.0		
Full-scale error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±5.5	LSB	AN000 to AN002 = AVCC0 – 0.2 V AN100 to AN102 = AVCC1 – 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±4.5		
Quantization error		Channel-dedicated sample-and-hold circuits in use		—	±0.5	—	LSB	
		Channel-dedicated sample-and-hold circuits not in use		—	±0.5	—		
Absolute accuracy	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		—	±3.0	±6.0	LSB	
		Channel-dedicated sample-and-hold circuits not in use		—	±2.5	±5.5		
	AN003, AN103			—	±2.5	±5.5		
	AN200 to AN211			—	±2.5	±5.5		
	AN216 to AN217			—	±2.5	±6.5		
DNL differential nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±1.0	±2.5	LSB	
		Channel-dedicated sample-and-hold circuits not in use		—	±1.0	±1.5		
INL integral nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±4.0	LSB	
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±2.5		
Holding time of the channel-dedicated sample-and-hold circuit				—	—	20	μs	
Dynamic range	AN000 to AN002	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC0 – 0.2	V	
	AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC1 – 0.2		

Note 1. When PCLKD was higher than 40 MHz, 1000 pF capacitors were placed in parallel with the 0.1-μF capacitors between AVCC0 and AVSS0, AVCC1 and AVSS1, and AVCC2 and AVSS2 for measurement of the A/D conversion characteristics.

Note 2. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

Table 2.45 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2)

Conditions: VCC = 2.7 to 4.5 V, 3.0 V ≤ AVCC0 = AVCC1 = AVCC2 < 4.5V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 40 MHz,
Source impedance = 1.0 kΩ

Item				Min.	Typ.	Max.	Unit	Test Conditions
Resolution				12	12	12	Bit	
Analog input capacitance				—	—	30	pF	
Conversion time*1 (Operation at PCLKD = 40 MHz)	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use	Constant sampling enabled	1.35	—	—	μs	• Sampling time: 18 PCLKD
			Constant sampling disabled	1.80	—	—		• Sampling time of channel-dedicated sample-and-hold circuits: 18 PCLKD • Sampling time: 18 PCLKD
		Channel-dedicated sample-and-hold circuits not in use		1.13	—	—		• Sampling time: 21 PCLKD
	AN003, AN103			1.13	—	—		• Sampling time: 21 PCLKD
	AN200 to AN211			1.20	—	—		• Sampling time: 24 PCLKD
	AN216 to AN217			1.28	—	—		• Sampling time: 27 PCLKD
Offset error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±7.5	LSB	AN000 to AN002, AN100 to AN102 = 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±6.5		
Full-scale error		Channel-dedicated sample-and-hold circuits in use		—	±1.5	±7.5		AN000 to AN002 = AVCC0 – 0.2 V AN100 to AN102 = AVCC1 – 0.2 V
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±6.5		
Quantization error		Channel-dedicated sample-and-hold circuits in use		—	±0.5	—		
		Channel-dedicated sample-and-hold circuits not in use		—	±0.5	—		
Absolute accuracy	AN000 to AN002, AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		—	±4.0	±8.0		
		Channel-dedicated sample-and-hold circuits not in use		—	±2.5	±7.0		
	AN003, AN103			—	±2.5	±7.0		
	AN200 to AN211			—	±2.5	±7.0		
	AN216 to AN217			—	±2.5	±8.0		
DNL differential nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±1.0	±4.5		
		Channel-dedicated sample-and-hold circuits not in use		—	±1.0	±3.5		
INL integral nonlinearity error		Channel-dedicated sample-and-hold circuits in use		—	±2.0	±5.0		
		Channel-dedicated sample-and-hold circuits not in use		—	±1.5	±3.5		
Channel-dedicated sample-and-hold characteristics of hold circuits				—	—	20	μs	
Dynamic range	AN000 to AN002	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC0 – 0.2	V	
	AN100 to AN102	Channel-dedicated sample-and-hold circuits in use		0.2	—	AVCC1 – 0.2		

Note 1. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

Table 2.46 A/D Internal Reference Voltage Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.20	1.25	1.30	V	

Note: The above specification values apply during normal operations.

2.6 Programmable Gain Amplifier Characteristics

Table 2.47 Programmable Gain Amplifier Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage	V_{IO}	—	3	8	mV	
Single-ended input voltage range	V_{ISR}	V_{OR} (min)/G	—	V_{OR} (max)/G	V	
Output voltage range	V_{OR}	0.10 × AVCCn	—	0.90 × AVCCn		G = 2.000 to 3.636
		0.15 × AVCCn	—	0.85 × AVCCn		G = 4.000 to 6.667
		0.20 × AVCCn	—	0.80 × AVCCn		G = 8.000 to 20.000
Gain	G	2.000	—	20.000	Linear gain	
Gain error	E_G	—	±0.5	±1.5	%	G = 2.000
		—	±0.5	±1.5		G = 2.500
		—	±0.5	±1.5		G = 3.077
		—	±0.5	±1.5		G = 3.636
		—	±0.6	±1.5		G = 4.000
		—	±0.6	±1.5		G = 4.444
		—	±0.7	±1.5		G = 5.000
		—	±0.7	±1.5		G = 6.667
		—	±0.7	±1.5		G = 8.000
		—	±0.7	±2.5		G = 10.000
		—	±1.1	±2.5		G = 13.333
		—	±1.3	±4.0		G = 20.000
Slew rate	SR	10	—	—	V/µs	
Operation stabilization time	t_{start}	—	—	5	µs	

n = 0 and 1

2.7 Comparator Characteristics

Table 2.48 Comparator Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input offset voltage	V_{IO}	—	8	15	mV	
Reference input voltage range	V_{ref}	0	—	AVCC1	V	CMPSEL1.CVRS[3:0] = 0100b, 1000b
		0	—	AVCC2		CMPSEL1.CVRS[3:0] = 0001b, 0010b
Response time	$t_{tot(r)}$	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	$t_{tot(f)}$	—	—	200		
Waiting time for stabilization following switching of the input	t_{cwait}	300	—	—		
Operation stabilization time	t_{cmp}	—	—	1	µs	

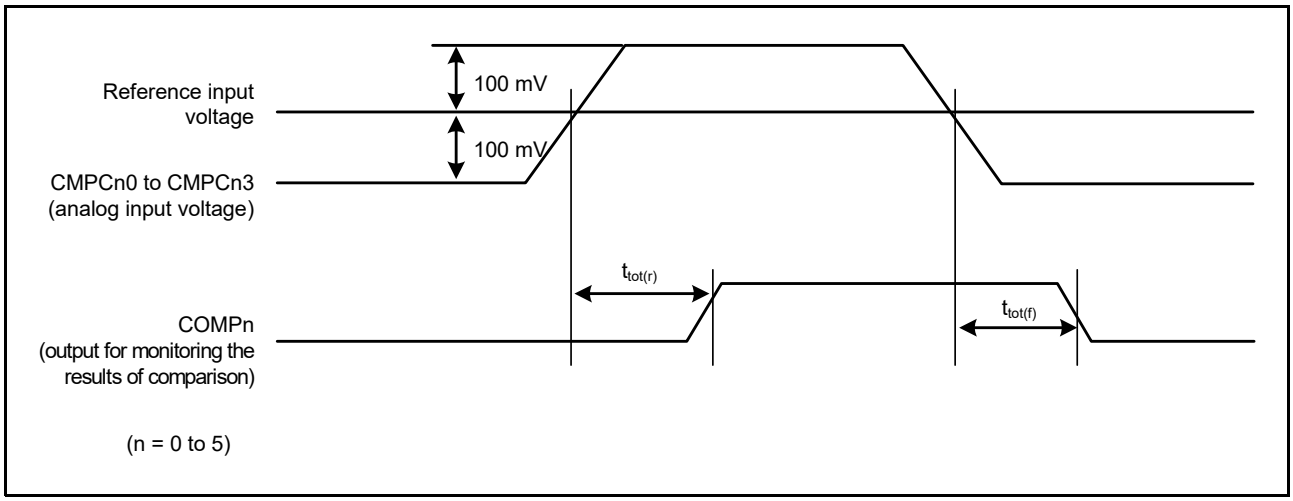


Figure 2.77 Comparator Response Time

2.8 D/A Conversion Characteristics

Table 2.49 D/A Conversion Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	12	12	12	Bit	
Absolute accuracy	—	—	±6.0	LSB	2-MΩ resistive load, 10-bit conversion
Differential nonlinearity error (DNL)	—	±1.0	±2.0	LSB	2-MΩ resistive load
Output resistance (R_o)	—	5.7	—	kΩ	
Conversion time	—	—	3	µs	20-pF capacitive load

2.9 Temperature Sensor Characteristics

Table 2.50 Temperature Sensor Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$,
PCLKB = PCLKD = 8 to 60 MHz

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1.0	—	°C	
Temperature slope	—	–2.0	—	mV/°C	
Output voltage	—	0.63	—	V	T_a = 25°C
Temperature sensor start time	—	—	200	µs	
Sampling time*1	3	—	—	µs	

Note 1. Set the S12AD2.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

2.10 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.51 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.46	2.58	2.70	V	Figure 2.78
	Voltage detection circuit (LVD0)	V_{det0_1}	4.04	4.22	4.40		Figure 2.79
		V_{det0_2}	2.71	2.83	2.95		
	Voltage detection circuit (LVD1)	V_{det1_0}	4.39	4.57	4.75		Figure 2.80
		V_{det1_1}	4.29	4.47	4.65		
		V_{det1_2}	4.14	4.32	4.50		
		V_{det1_3}	2.81	2.93	3.05		
		V_{det1_4}	2.76	2.88	3.00		
	Voltage detection circuit (LVD2)	V_{det2_0}	4.39	4.57	4.75		Figure 2.81
		V_{det2_1}	4.29	4.47	4.65		
		V_{det2_2}	4.14	4.32	4.50		
		V_{det2_3}	2.81	2.93	3.05		
		V_{det2_4}	2.76	2.88	3.00		
Internal reset time	Power-on reset time	t_{POR}	—	15.5	—	ms	Figure 2.78
	LVD0 reset time	t_{LVD0}	—	0.70	—		Figure 2.79
	LVD1 reset time	t_{LVD1}	—	0.57	—		Figure 2.80
	LVD2 reset time	t_{LVD2}	—	0.57	—		Figure 2.81
Minimum VCC down time		t_{VOFF}	200	—	—	µs	Figure 2.78, Figure 2.79
Response delay time		t_{det}	—	—	200	µs	Figure 2.78 to Figure 2.81
LVD operation stabilization time (after LVD is enabled)		$T_{d(E-A)}$	—	—	20	µs	Figure 2.80, Figure 2.81
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

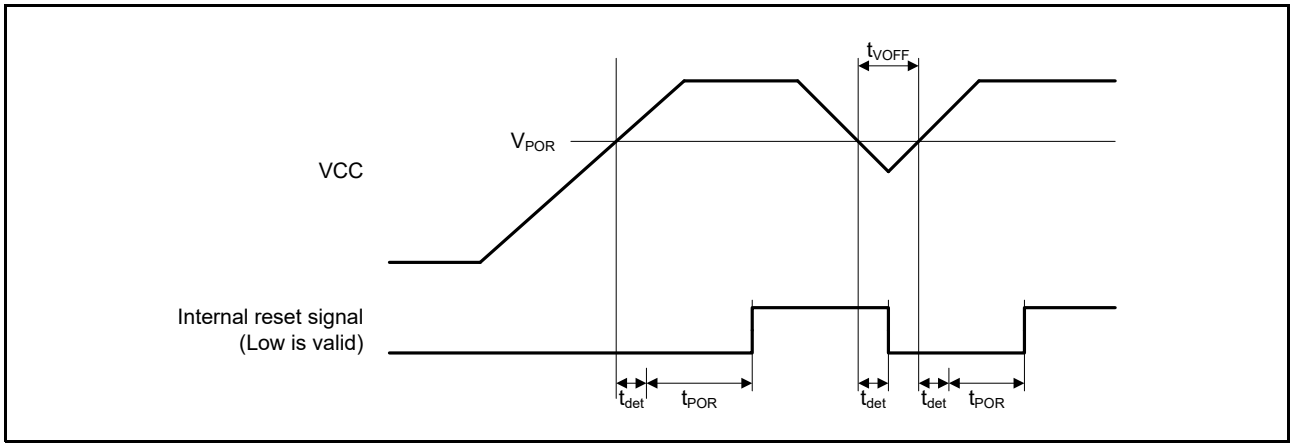


Figure 2.78 Power-on Reset Timing

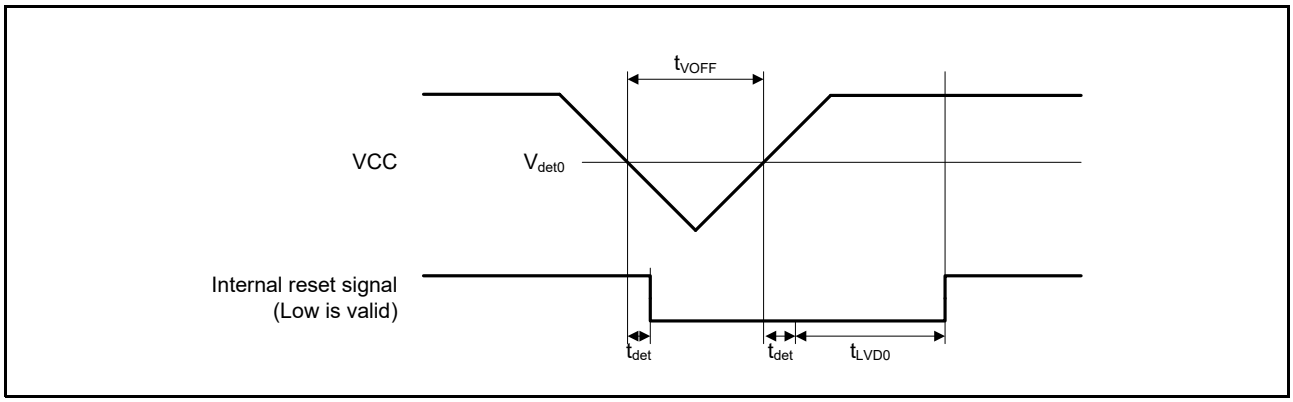


Figure 2.79 Voltage Detection Circuit Timing (V_{det0})

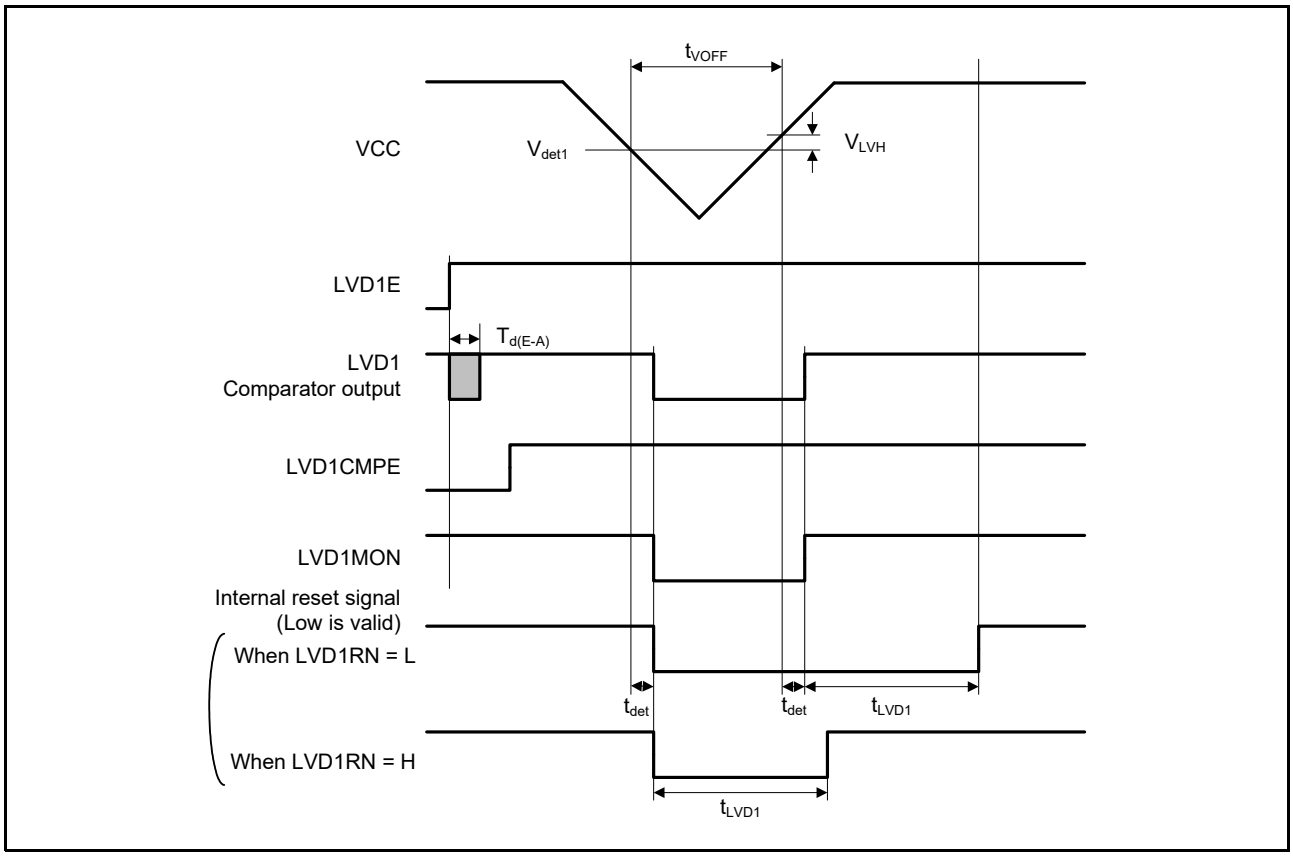


Figure 2.80 Voltage Detection Circuit Timing (V_{det1})

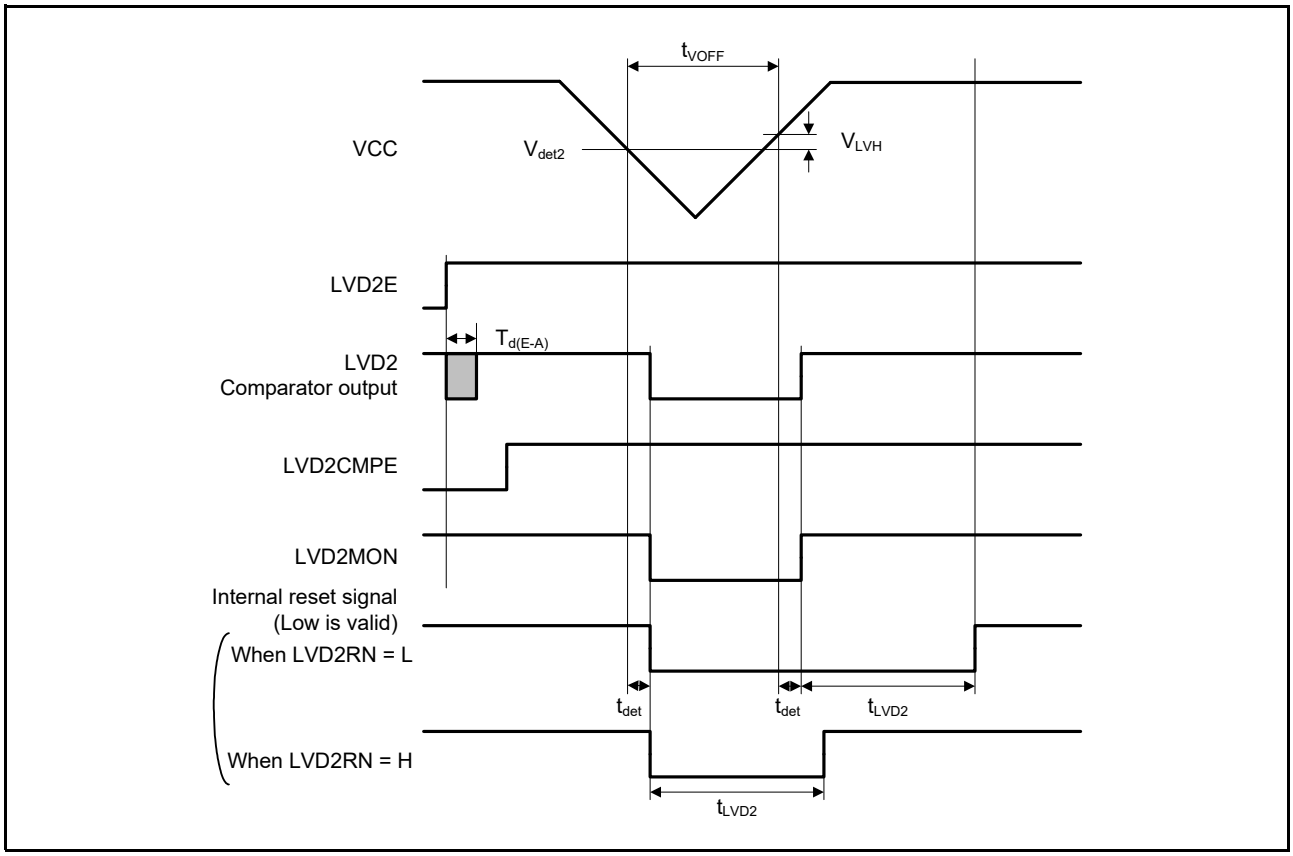


Figure 2.81 Voltage Detection Circuit Timing (V_{det2})

2.11 Oscillation Stop Detection Timing

Table 2.52 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.82

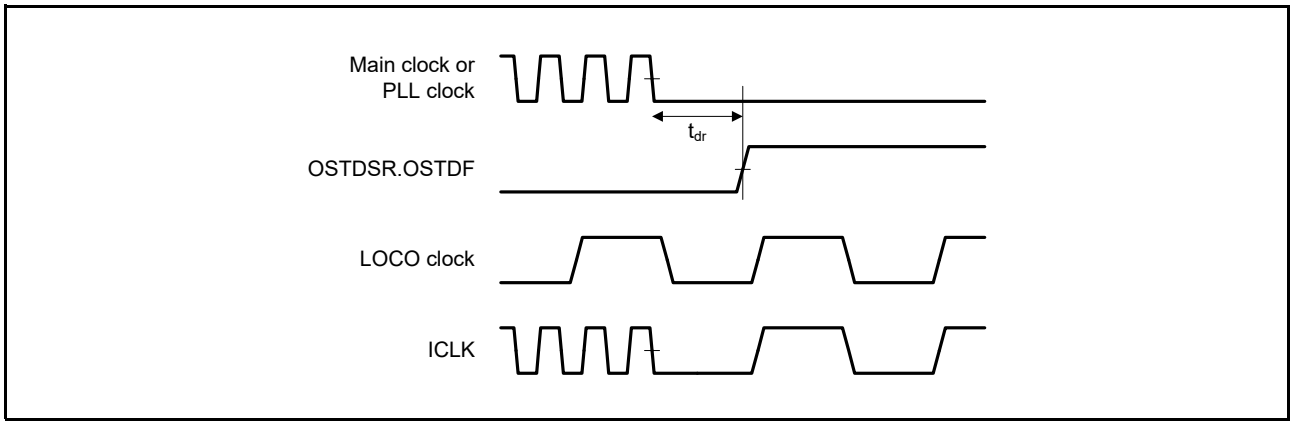


Figure 2.82 Oscillation Stop Detection Timing

2.12 Flash Memory Characteristics

Table 2.53 Code Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Program time (N_{PEC} ≤ 100 cycles)	128 bytes	t_{P128}	—	0.66	11	—	0.3	5	ms	
	8 Kbytes	t_{P8K}	—	37	176	—	17	80		
	32 Kbytes	t_{P32K}	—	150	704	—	68	320		
Program time (N_{PEC} > 100 cycles)	128 bytes	t_{P128}	—	0.71	13	—	0.32	6	ms	
	8 Kbytes	t_{P8K}	—	46	212	—	21	96		
	32 Kbytes	t_{P32K}	—	185	848	—	84	384		
Erase time (N_{PEC} ≤ 100 cycles)	4 Kbytes	t_{E4K}	—	43	108	—	24	60	ms	
	32 Kbytes	t_{E32K}	—	284	864	—	158	480		
Erase time (N_{PEC} > 100 cycles)	4 Kbytes	t_{E4K}	—	50	130	—	28	72	ms	
	32 Kbytes	t_{E32K}	—	338	864	—	188	480		
Program/erase cycles*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Cycles	
Program suspend latency		t_{SPD}	—	—	264	—	—	120	µs	
Primary erase suspend latency in suspend priority mode		t_{SESD1}	—	—	216	—	—	120		
Secondary erase suspend latency in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Erase suspend latency in erase priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data retention*3, *4		t_{DRP}	20	—	—	20	—	—	Year	T_a ≤ 85°C
			10	—	—	10	—	—		T_a ≤ 105°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 256-byte program is performed 32 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 2.54 Data Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Program time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
Erase time	64 bytes	t_{DE64}	—	3.1	18	—	1.7	10		
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	µs	
	64 bytes	t_{DBC64}	—	—	280	—	—	100		
	2 Kbytes	t_{DBC2K}	—	—	6160	—	—	2200		
Program/erase cycles*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	Cycles	
Program suspend latency		t_{DSPD}	—	—	264	—	—	120	µs	
Primary erase suspend latency in suspend priority mode		t_{DSESD1}	—	—	216	—	—	120		
Secondary erase suspend latency in suspend priority mode		t_{DSESD2}	—	—	300	—	—	300		
Erase suspend latency in erase priority mode		t_{DSEED}	—	—	300	—	—	300		
Forced stop command		t_{FD}	—	—	32	—	—	20		
Data retention*3, *4		t_{DDRP}	20	—	—	20	—	—	Year	$T_a \leq 85°C$
			10	—	—	10	—	—		$T_a \leq 105°C$

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

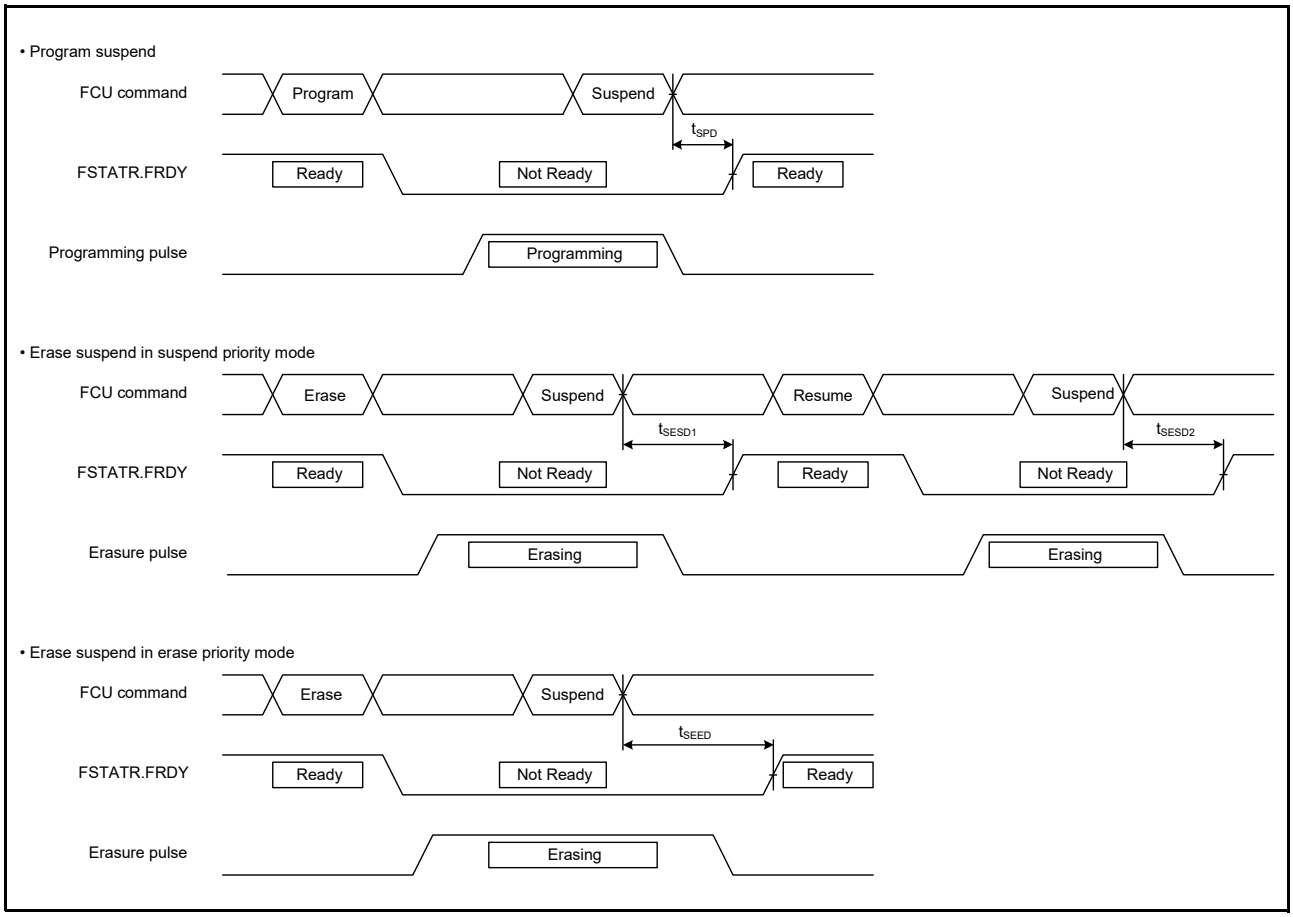


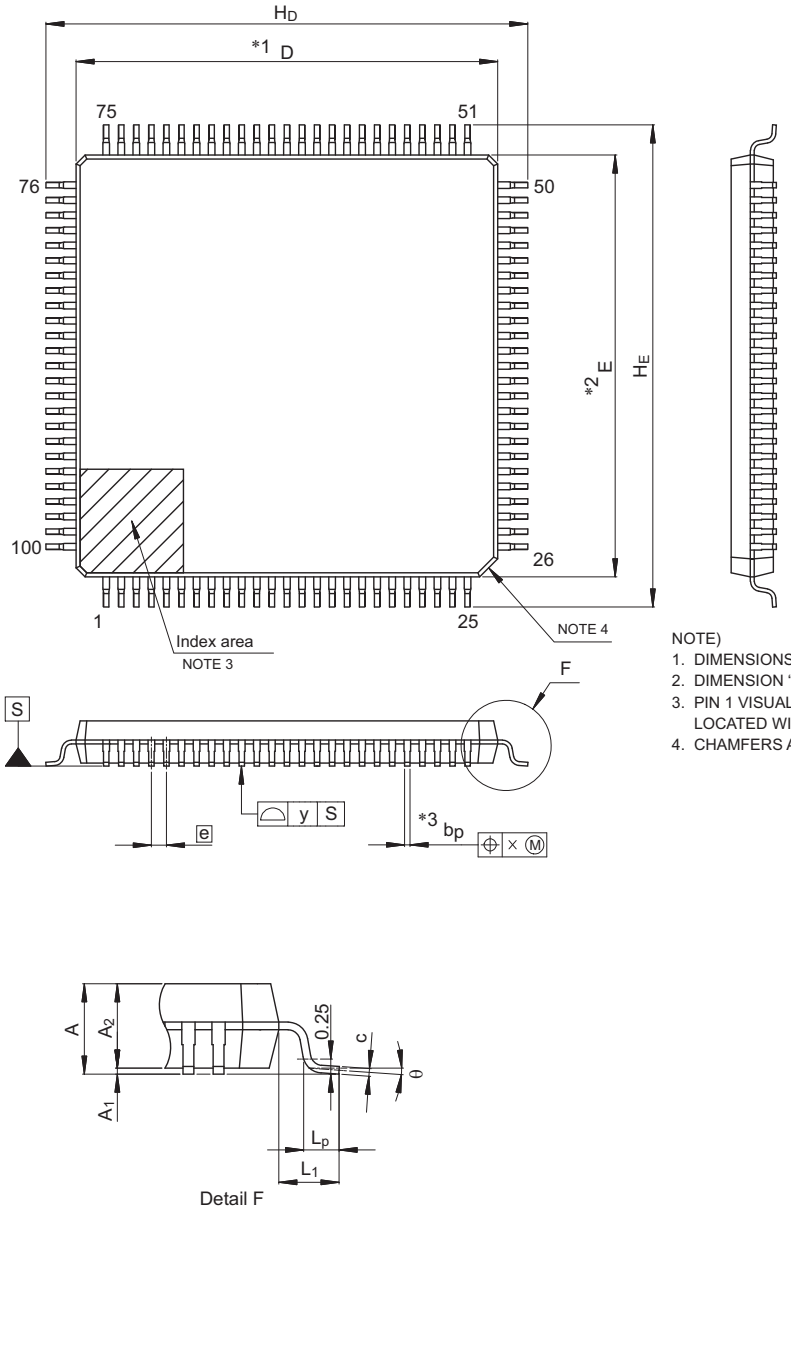
Figure 2.83 Flash Memory Program/Erase Suspend Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



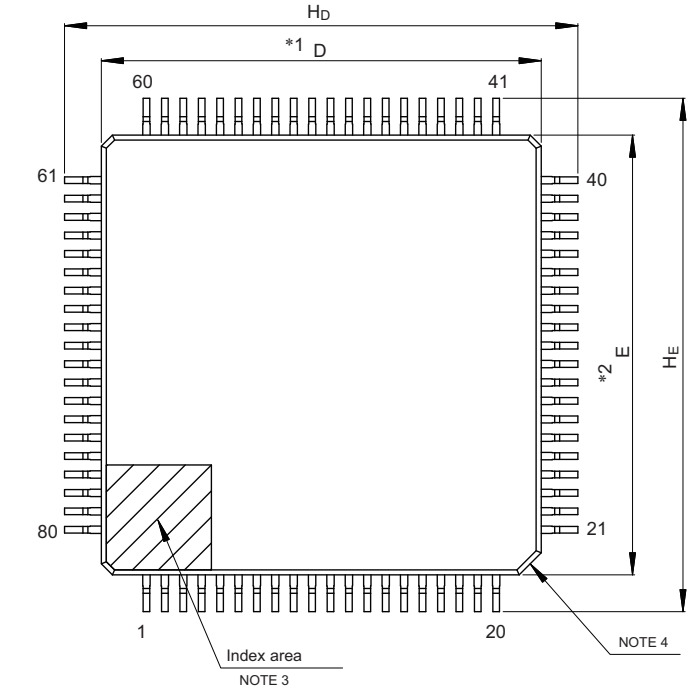
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

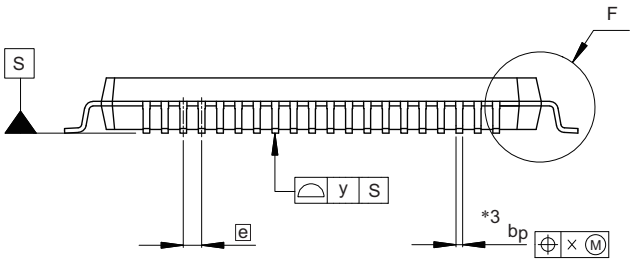
Figure A 100-Pin LFQFP (PLQP0100KB-B)

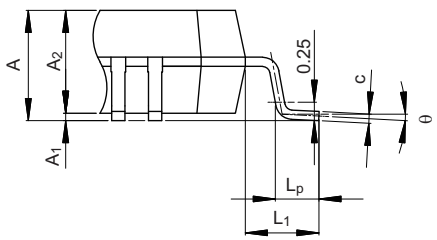
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





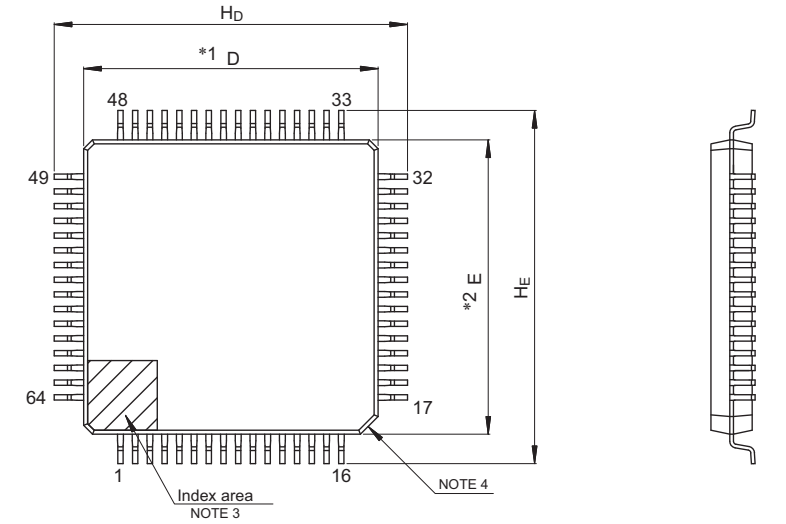
Detail F

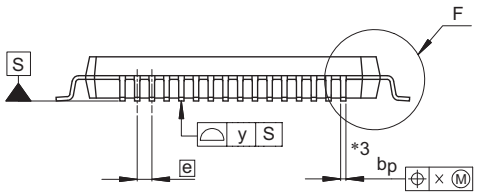
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

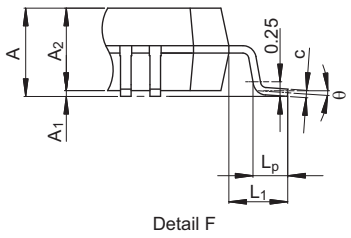
Figure B 80-Pin LFQFP (PLQP0080KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







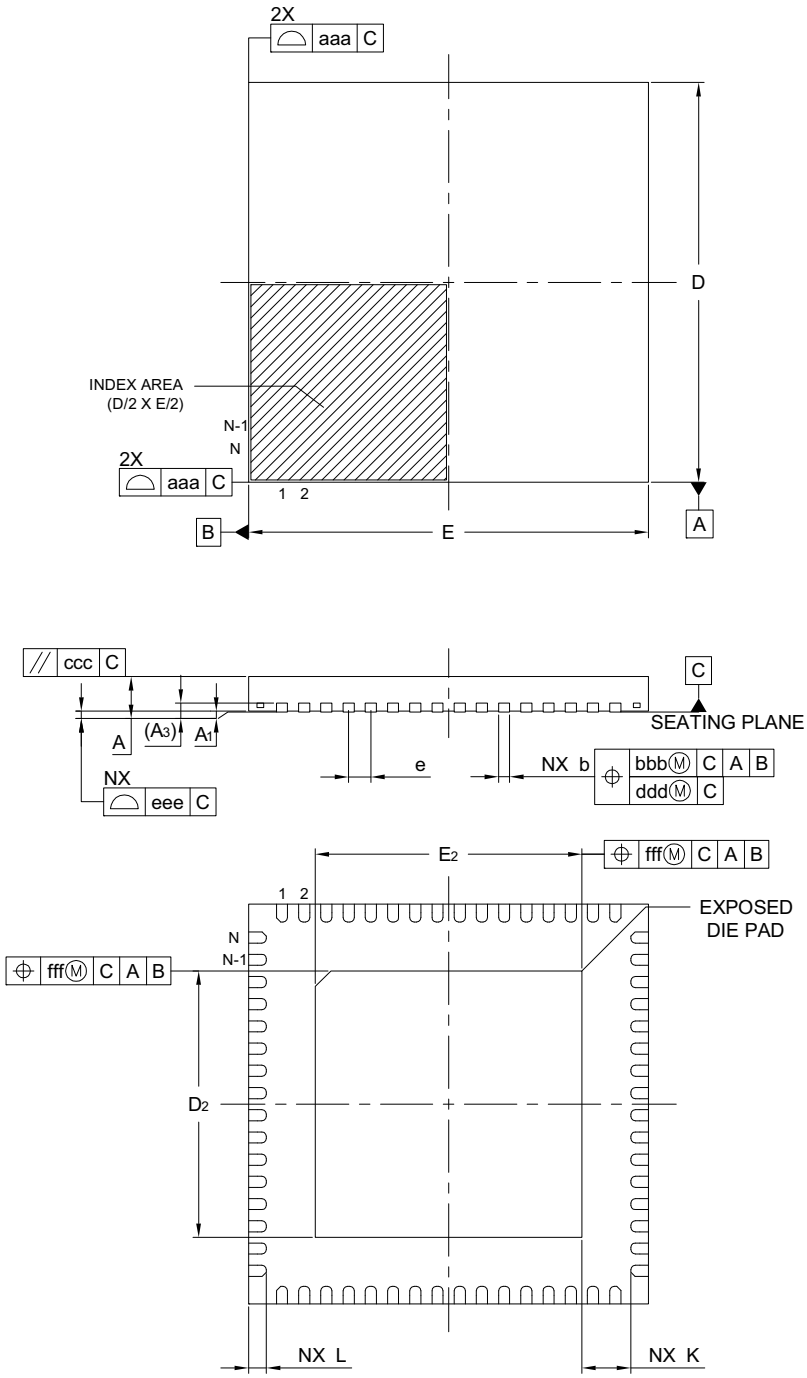
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure C 64-Pin LFQFP (PLQP0064KB-C)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN064-9x9-0.50	PWQN0064KF-A	0.17

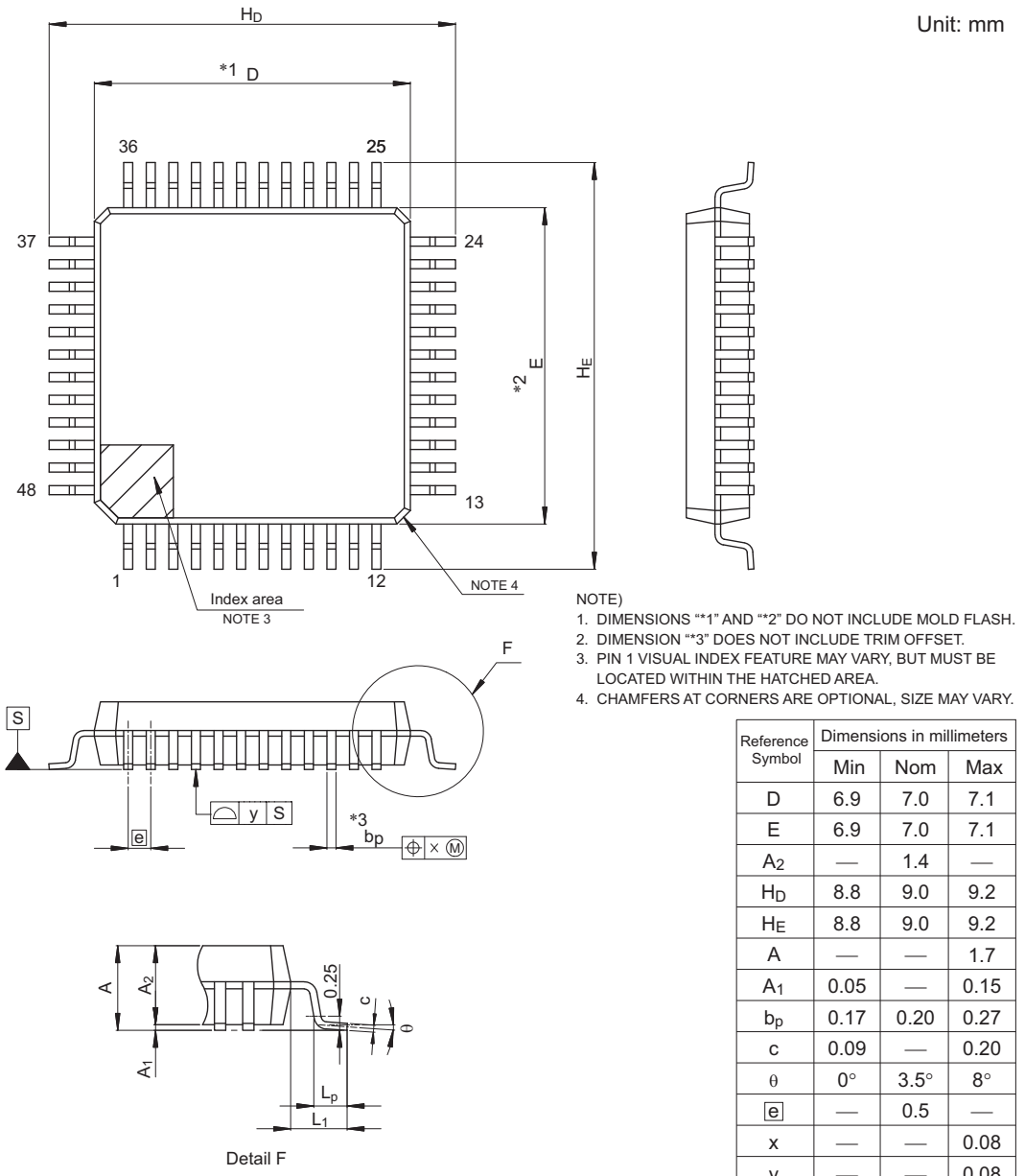


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		9.00 BSC	
E		9.00 BSC	
e		0.50 BSC	
N		64	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	5.95	6.00	6.05
E_2	5.95	6.00	6.05
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
fff	—	—	0.10

Figure D 64-Pin HWQFN (PWQN0064KF-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm

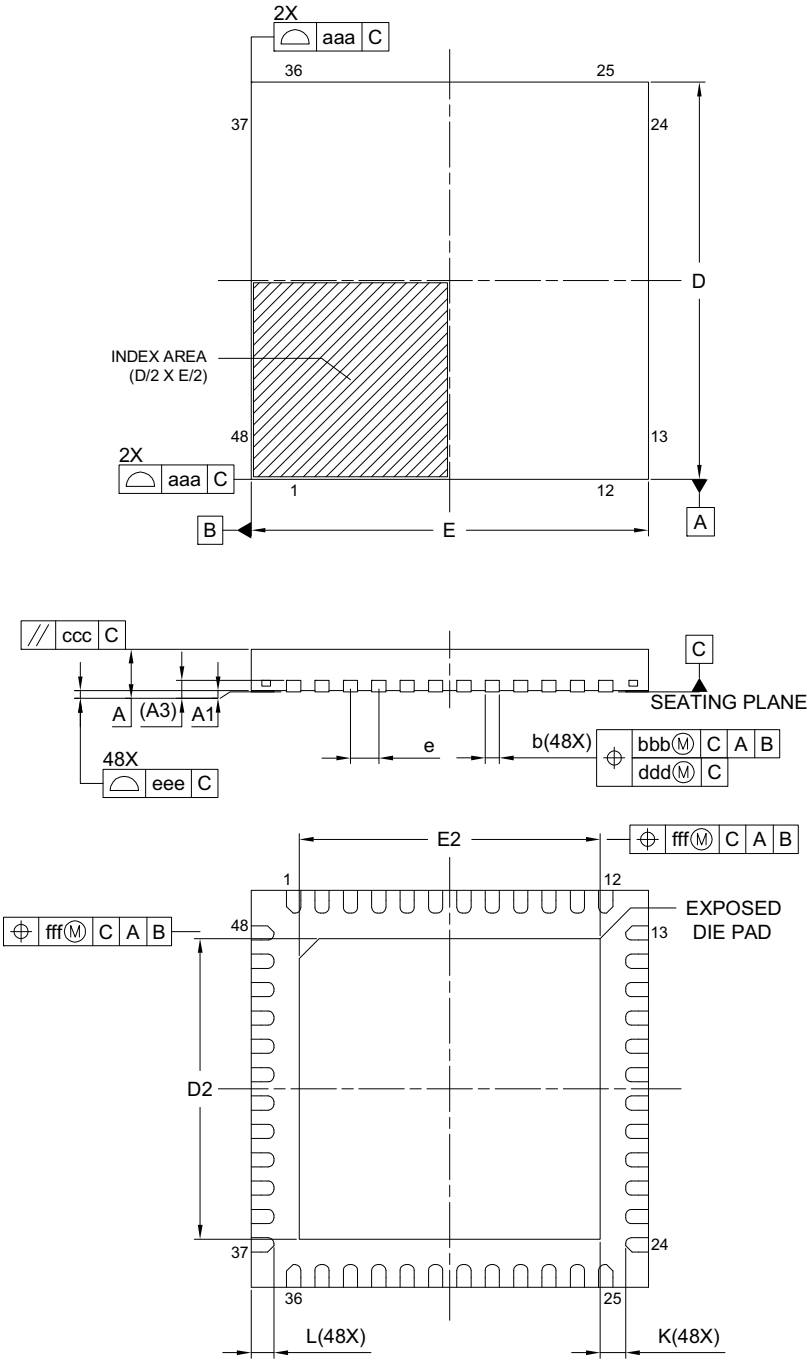


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure E 48-Pin LFQFP (PLQP0048KB-B)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure F 48-Pin HWQFN (PWQN0048KC-A)

REVISION HISTORY	RX26T Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jan 16, 2023	—	First edition, issued	
1.01	Mar 01, 2023	Features		
		1	Package, changed	
		1. Overview		
		13 to 15	Table 1.3 List of Products, changed	
		2. Electrical Characteristics		
		64	Table 2.10 Permissible Output Currents, changed	
		67	Table 2.13 Thermal Resistance Value (Reference), changed	
1.10	Aug 10, 2023	1. Overview		
		10	Table 1.1 Outline of Specifications (9/9), changed	
		13 to 15	Table 1.3 List of Products, changed	
		16	Figure 1.1 How to Read the Product Part Number, changed	
		2. Electrical Characteristics		
		60	Table 2.6 DC Characteristics (3) (Products with 64 Kbytes of RAM), changed	
		61	Table 2.7 DC Characteristics (3) (Products with 48 Kbytes of RAM), changed	

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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